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D2.6

EoT Device with Factor Form Board

1. DOCUMENT INFORMATION

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6. ABSTRACT

The EoT device with the factor-form board consists of a custom-designed 10-layer high density PCB that is optimised for size and power efficiency. All processing and control is controlled by the low-power Myriad2 MA2150 VPU. The primary visual sensor is a 1x1x1.7mm NanEye2D sensor from Awaiba, which is capable of capturing 250x250 pixel images. This is a module package CMOS image sensor and integrated lens that is fully self-timed, consuming less than 5mW at 60 frames per second (fps). Additional peripherals such as a tri-axial gyroscope, tri-axial accelerometer, magnetometer, and microphone enable a cascade filtering approach for 'interesting' event detection and reaction. Based on the sensor data and the information extracted from visual processing and neural inference, decisions coupled with relevant metadata can be communicated over an integrated Wi-Fi module to external devices or to the cloud. In personal assistant use-cases, audio cues for prompting and notification are enabled via a full on-board audio codec. Integrated level shifters expose motor control pins for direct, yet generic, robotic control (GPIOs, PWMs, I2C, and UART) without the need for external components. By combining Myriad2, NanEye, low-power board design and energy efficient component selection, the EoT platform can run for up to 24 hours from a fully charged Lithium-ion Polymer (Li-Po) battery. USB and micro-SD functionality support rapid development and data logging modalities.

7. EOT FORM-FACTOR BOARD FEATURES

Following from deliverable document EoT_D2.5, where we described the history and process of the EoT form-factor board (FfBoard) design, we are going to present the updated information regarding the board design and device by itself in this document. As mentioned in there, the focus of FfBoard design has been to minimize the board size as much as possible by removing unnecessary components and substituting the others with smaller and more efficient ones as feasible. As mentioned, we prioritized the design factors such as power/size/price, while the one with the lowest priority was not pushed too far. According to the EoT project's proposal, the target size for FfBoard has been to achieve 1.5x3 cm (approx.). Such a small size has proven a really challenging objective. In addition, we planned to design a non-stackable form-factor board and as small as possible by cleverly selecting the components and by increasing the EoT FfBoard layers. Figure 6-1 shows the EoT FfBoard block diagram according to the finalised spec.

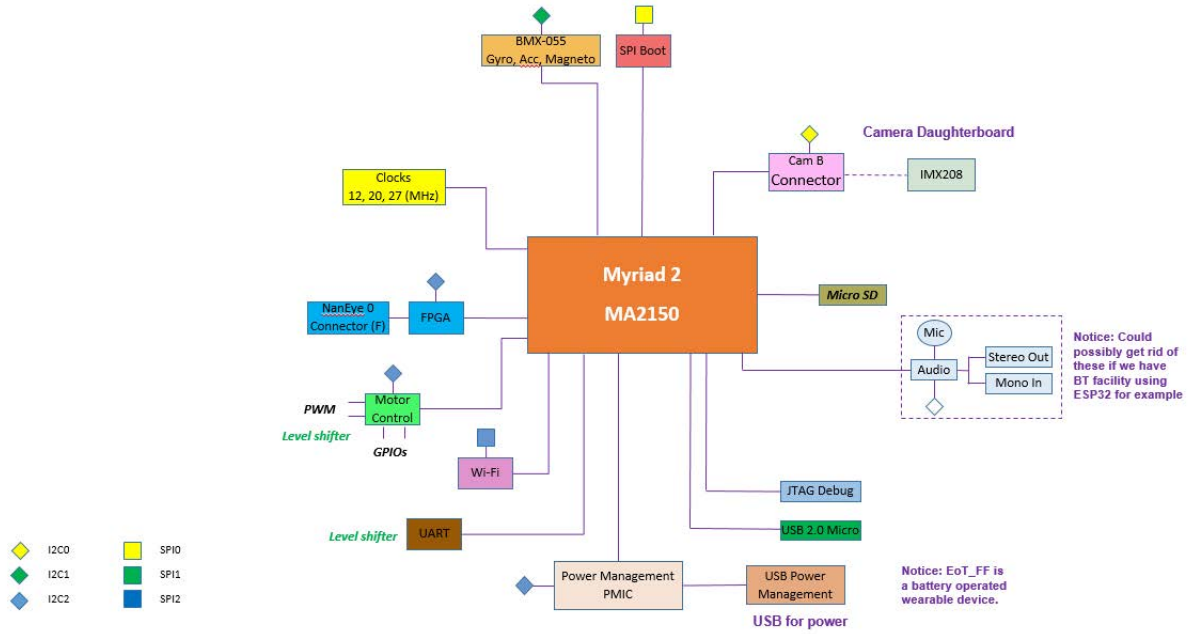


Figure 6-1: EoT FfBoard block diagram.

EoT Form Factor Board Hardware Features

In this section the main features and capabilities of the EoT wearable device will be reviewed.

7.1.1. Vision Processing Unit (VPU)

The EoT device is based on the Myriad 2 VPU (see Figure 6-2). It supports two trillion 16-bit operations per second at a power consumption of 500mW. The architecture is based on 12 128-bit very long instruction word "SHAVE" processors and two 32-bit RISC processors (LeonOS and LeonRT). The chip includes 2-Mbytes of on-chip memory and 400-Gbytes per second of sustained internal memory bandwidth.

The off-chip memory requirement is for up 8-Gbits of 2 Vy 32 LPDDR2 or LPDDR3 DRAM capable of up to 1,066MHz operation. It supports up to six full HD 60 frames per second camera inputs simultaneously via MIPI lanes.

Given its highly parallelized data processing architecture and on-chip memory fabric, Myriad-2 can achieve high-performance processing with low latency.

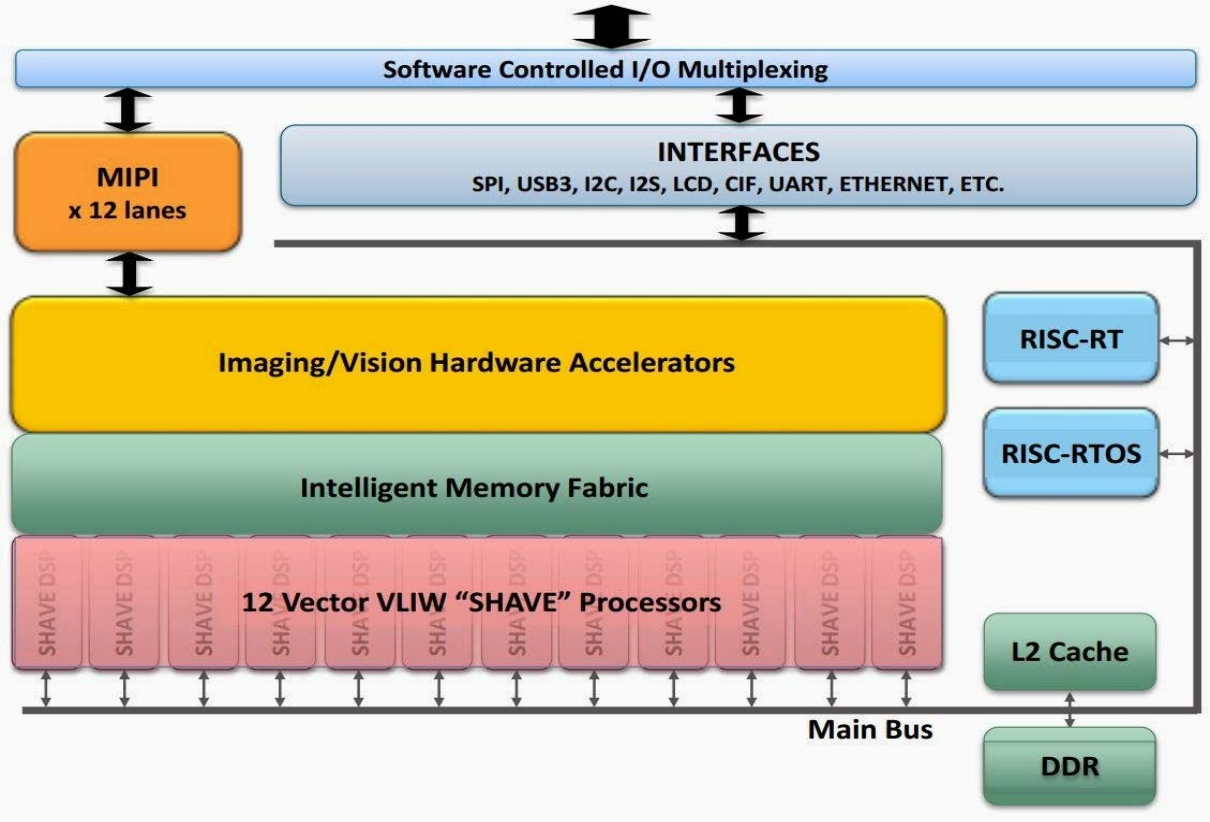


Figure 6-2 Myriad 2 Block Diagram.

The MA2150, which is from the MA2x5x Myriad family, is used in EoT wearable device with form-factor board. A brief overview of the Myriad2 common features is presented below:

- 12 x SHAVE VLIW vector processor, 2 x RISC processor
- There is 2 MB of on-chip RAM (CMX)
- 128/512 MB of in-package stacked DDR
- LEON OS has 256 KB L2 cache memory
- LEON RT has 32 KB L2 cache memory
- Exceptionally high sustainable on-chip bandwidth
- SIPP Image Signal Processing hardware accelerators
- Wide range of IO peripherals interfaces, such as SPI (3), I2C (3), I2S (3), SDIO, Ethernet, USB
- Imaging interfaces, such as MIPI (6), CIF (2), LCD.

MA2x5x is the second series of the Myriad 2 family with four members (MA2150/MA2155/MA2450/MA2455) and the following specific features:

- 600 MHz system clock
- USB 3.0 operation
- Dual voltage SDIO 1.8 V & 3.3 V
- USB boot mode
- IQ and performance improvements in SIPP ISP pipeline – 600 MPixels/s throughput
- On-die temperature sensors

- 6 simultaneous camera support
- 128 MB of in-package stacked LP-DDR2 @ 533 MHz (MA215x)
- 512 MB of in-package stacked LP-DDR3 @ 933 MHz (MA245x)
- Secure boot mode (MA2x55)
- Low power state improvements

The MA2150 architecture block diagram can be found on Figure 6-3.

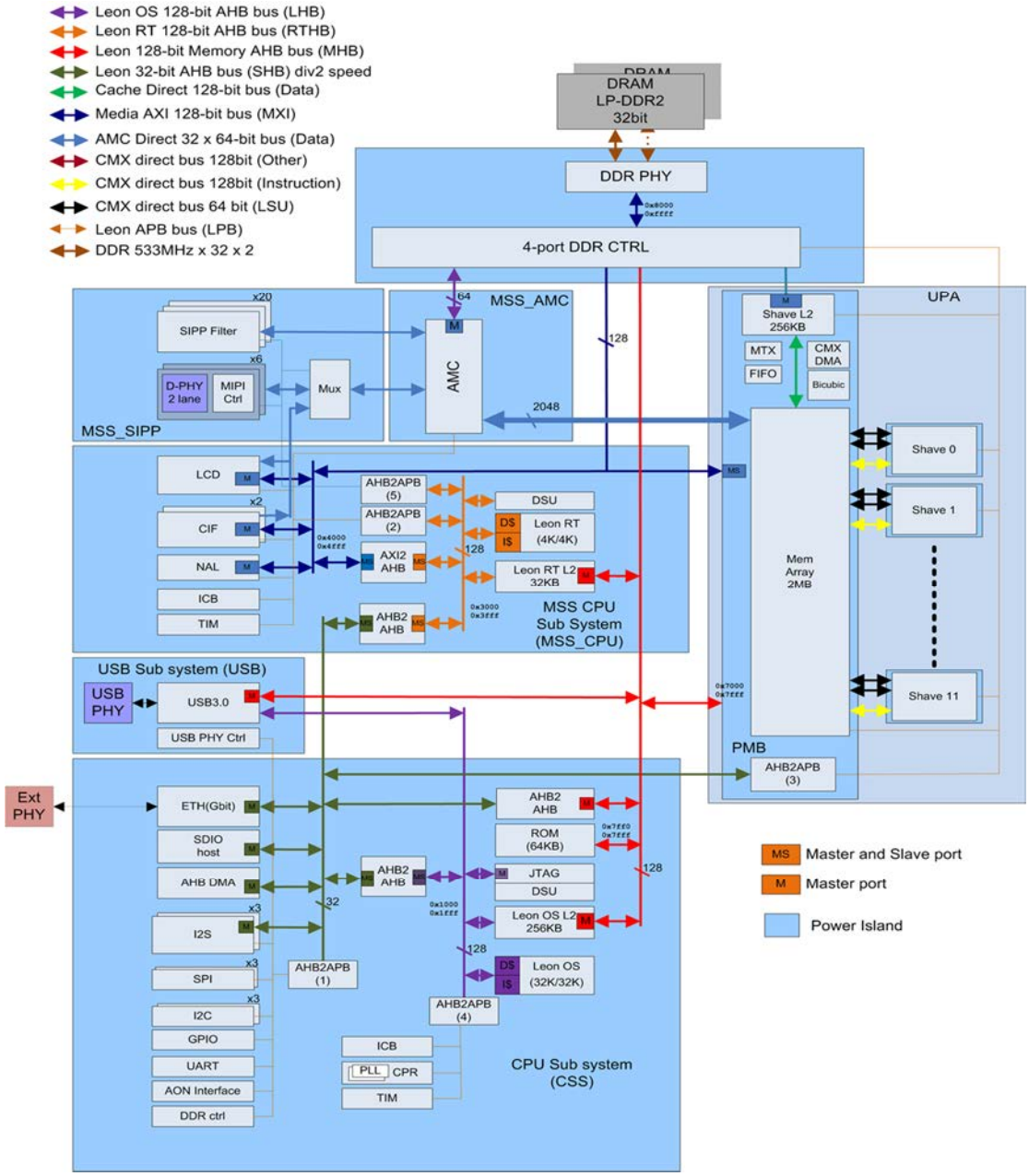


Figure 6-3 MA2150 Architecture Diagram – Block level

The operating system used by the EoT device is RTEMS. This OS is designed for real-time, embedded systems and supports various open API standards. RTEMS supports the POSIX standard of Linux. It also provides a port of the FreeBSD TCP/IP stack and support for several filesystems such as the FAT filesystem.

RTEMS does not provide any form of memory management or processes. In POSIX terminology, it implements a single process, multithreaded environment.

This OS is distributed under a modified GNU General Public License (GPL), allowing linking RTEMS objects with other files without needing the full executable to be covered by the GPL.

7.1.2. Myriad 2 programming paradigms

7.1.2.1. Standard programming paradigm

This first approach concerning Myriad 2 is focused on using the implemented SIPP pipeline. SIPP is a programming paradigm that involves a graph of connected filters in which data is streamed from one filter to the next, on a scanline-by-scanline basis. Images are consumed in raster order not requiring DDR accesses (other than accessing any pipeline input or output images located in DDR, using DMA copies to/from local memory). In addition to the performance and power benefits of avoiding DDR accesses, the design can also reduce hardware costs, allowing stacked DDR to be omitted for certain types of applications.

As the standard programming paradigm for Myriad, this approach involves using RTEMS running on LeonOS and the SIPP scheduler on LeonRT. The advantage of this paradigm is that it provides parallelization in an easy to use environment. The SIPP scheduler itself is able to ensure parallel pipeline configurations for managing the HW filters and exterior interfaces with a low footprint so as to ensure LeonRT optimized utilization. The SIPP used number of SHAVEs is configurable, so any extra number of SHAVEs not used for line based pipelines will remain free to be used by the RTEMS operating system running on LeonOS for various other purposes including computer vision algorithms.

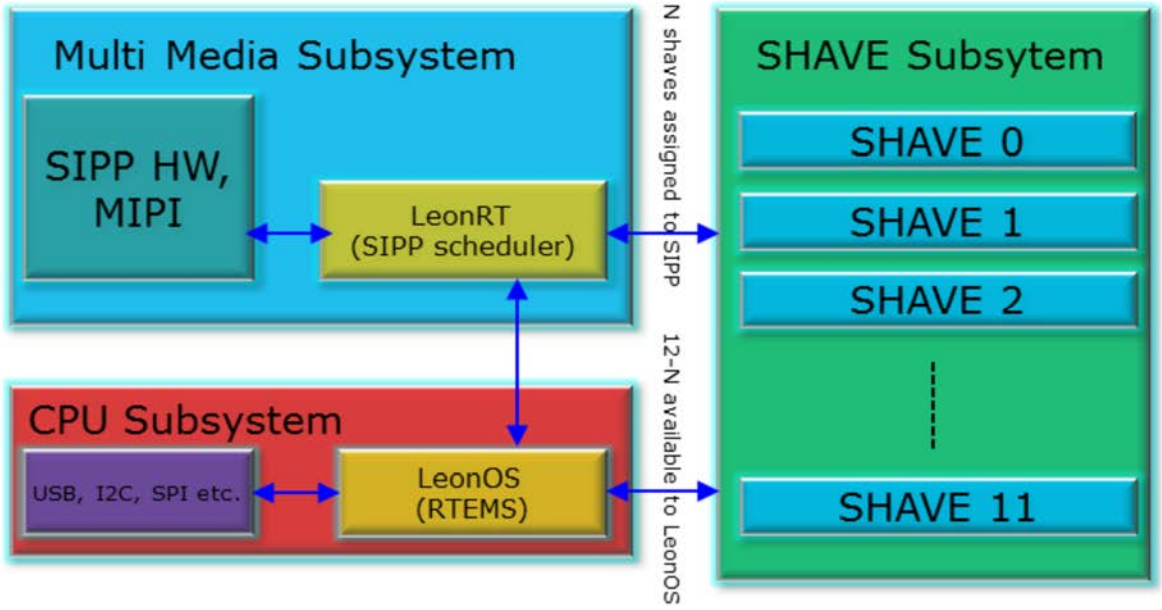


Figure 6-4: Standard programming paradigm diagram.

7.1.2.2. The One Leon programming paradigm

Some applications might not require heavy line based processing. Such applications might choose to completely switch OFF the LeonRT processor and instead only use LeonOS with (or without) RTEMS. HW filters may still be used.

Using this programming paradigm, Leon OS would control all of the applications running on the 12 SHAVE cores.

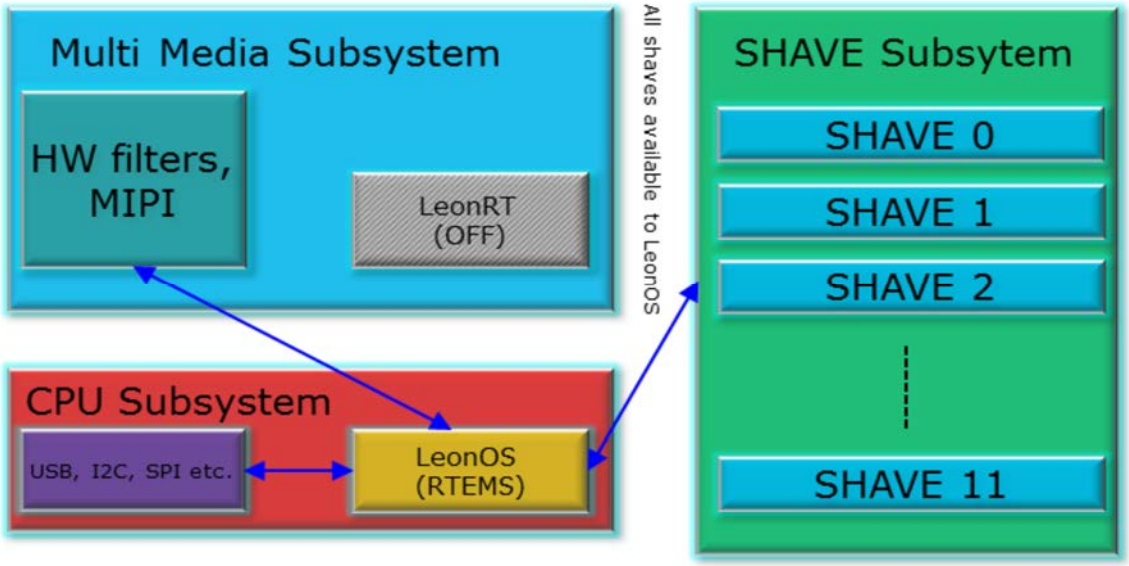


Figure 6-5: One Leon programming paradigm diagram

7.1.2.3. Bare metal programming paradigm

A bare metal programming paradigm will also be supported by the MDK build system. This will allow developer to use both LEON cores without any operating system, only minimal schedulers running to control the pipelines application. This paradigm requires more integration efforts but allows developers to write applications which will not be affected by any operating system overhead.

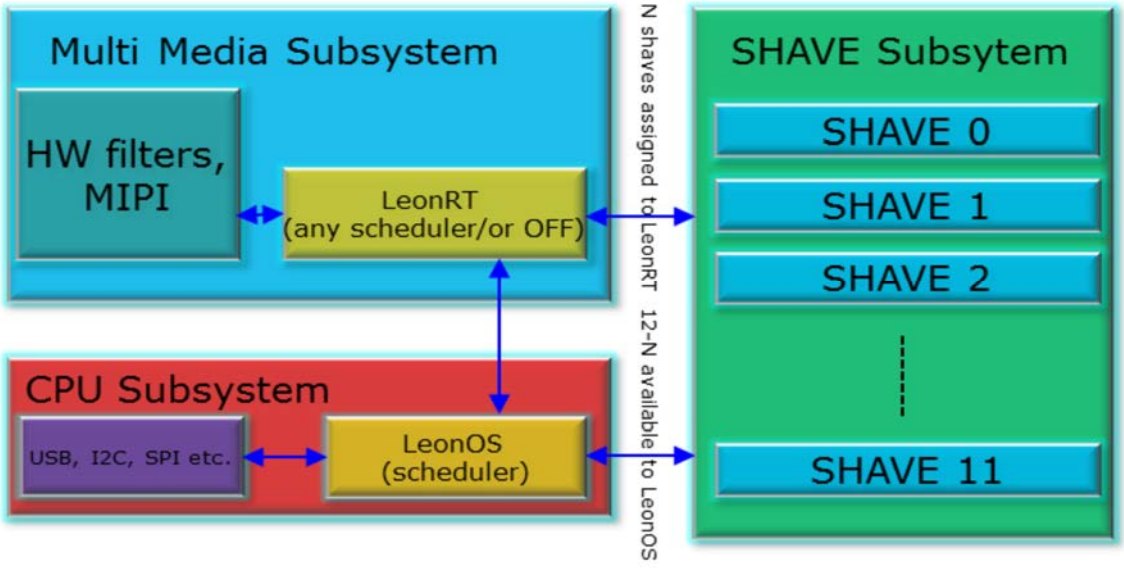


Figure 6-6. Bare metal programming paradigm diagram

7.1.2.4. Selected paradigm

With regard to EoT, "one Leon programming paradigm" has been the selected paradigm. This approach allows to deactivate the LeonRT when not necessary, reducing the energy consumption.

7.1.3. EoT firmware

The EoT firmware is divided into the following modules:

- **Wi-Fi data transfer:** This module provides a layer of functions for managing the Wi-Fi chip.
- **Camera interface:** This module provides software on top of the camera driver for retrieving frames.
- **Video streaming:** This module provides an application for streaming the video captured through the camera interface.
- **Input buttons/DIP switches:** This module provides functionality to check the status of the DIP switches and user pushbuttons in the board. It also provides functions to turn the two user LEDs on/off.
- **SD card management:** This module provides the functionality for reading and writing data to the SD card.
- **Bootloader:** This module allows the EoT board to be started in control mode or to run another uploaded application.
- **Control mode API, embedded side:** This application is used for configuring and managing the EoT board.
- **Audio input & output:** This module provides the functionality for reproducing a stored audio file.
- **Computer vision - CNN:** This module includes an implementation of Convolutional Neural Networks for the EoT device.
- **Computer vision - Color histogram matching:** This module includes an implementation of color histogram matching algorithms for the EoT device.
- **Computer vision - Keypoint matching:** This module includes an implementation of keypoint matching algorithms for the EoT device
- **Computer vision - Rotation-invariant face detector:** This module includes an implementation of rotation-invariant face detection algorithms for the EoT device.
- **Computer vision - Sparse optical flow (LK point tracking):** This module includes an implementation of sparse optical flow algorithms for the EoT device.
- **Power management:** This module can be used in an application for placing the Myriad chip into a low-power state.
- **Control mode API, Desktop:** This is a JAVA library and application for desktop PC that provides functions for interaction with the "Control Mode API embedded side" module.
- **Control mode API, Android:** This is an Android library and application for mobile phones that provides functions for interaction with the "Control Mode API embedded side" module.
- **Other vision libraries:** This module provides ports of several pre-existing vision libraries to the EoT platform.
- **Motor control:** This module provides communication with motors.

Figure 6-7 shows the EoT firmware structure.

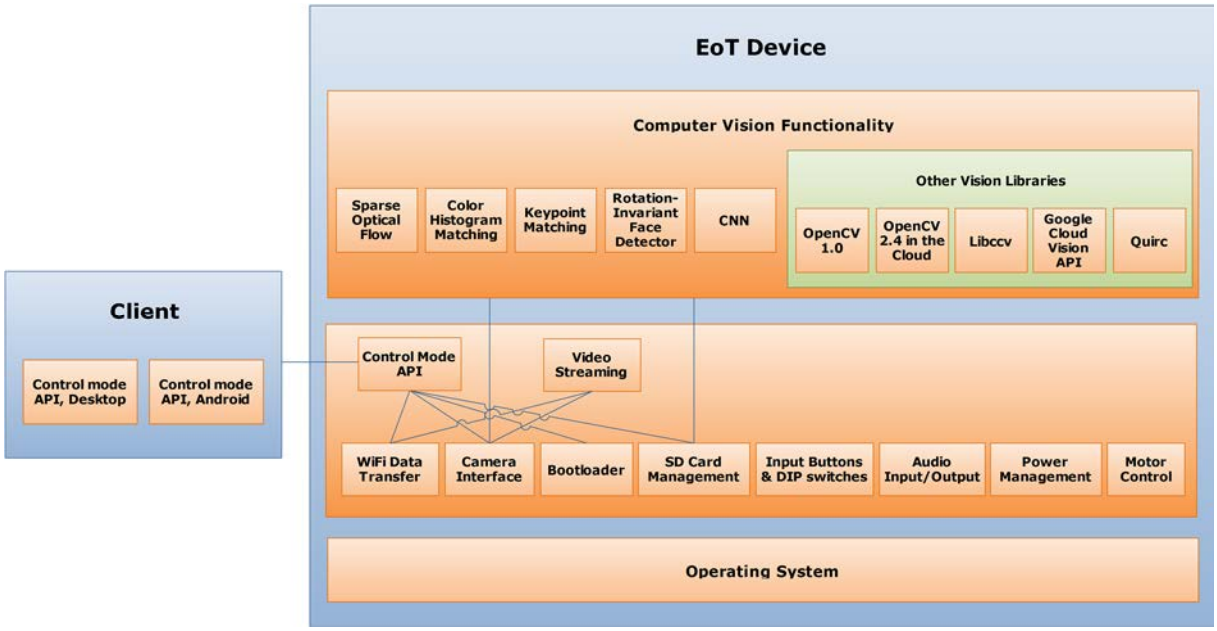


Figure 6-7 EoT firmware structure.

7.1.4. Wi-Fi connectivity

When designing a device on a power budget, computer vision could be previously attempted only with basic tasks. EoT's advantage of using energy-optimized processing is two-fold. On the one hand consumption is reduced in the most power-hungry element. On the other hand, since more complex tasks can be performed the inferred results will be more succinct, which in turn means less bandwidth usage and therefore less networking energy. Figure 6-8 shows where EoT stands on energy consumption.

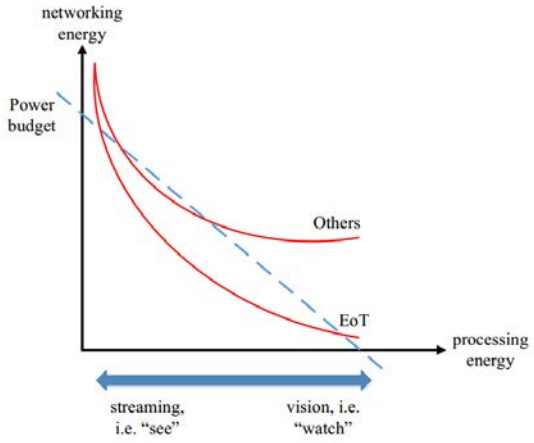
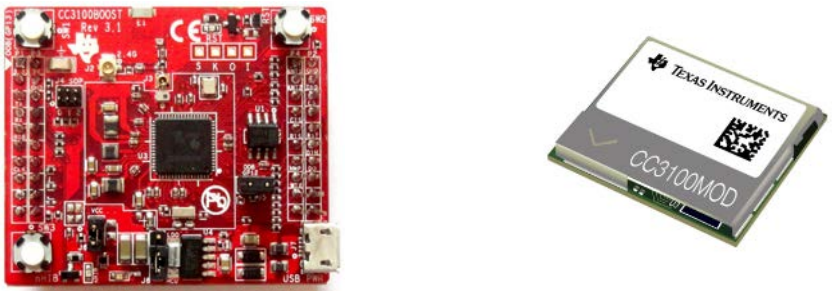


Figure 6-8: Vision on a power budget.

Even though energy-efficient processing is crucial, EoT needs appropriate network protocols. It aims at being both interoperable and flexible, so video streaming must be possible (although not always desirable). EoT uses TCP/IP over Wi-Fi, since it supports video streaming and is widely deployed. MOVIDIUS-UCLM selected the TI CC3100 Wi-Fi module (see Figure 6-9(a)) for EoT project carefully among a number of candidates. It is a low-power (4 μA hibernate, 115 μA deep sleep, 50-230 μA active), easy-to-use, and quick design Wi-Fi module created for the Internet of Things (IoT) with all required protocols integrated.



(a) (b)

Figure 6-9: Wi-Fi TI CC3100BOOST.

For the EoT device with the form-factor board the small canned (see Figure 6-9(b)) version of TI's module has been used. The data transfer using this Wi-Fi module is handled using the SPI driver. This software will provide a layer of functions for creating an ad-hoc Wi-Fi network, establishing a connection with another device, sending/receiving data (of any kind) and closing the connection. The CC3100MOD can create an ad-hoc network and has security and encryption (WPA2). The ad-hoc Wi-Fi will allow connection with the external configuration computer even without Wi-Fi infrastructure.

Since the SSID is public, an additional security feature shall be used: a network password. When using WPA, the password is a string of between 8 and 63 characters. When in place, this password will be needed to use the EoT device. The password is stored in the CC3100MOD's flash memory and can be eventually changed (or removed) from the Control mode (see below).

The original DoW[1] mentioned the use of the MQTT protocol for lightweight communication (over TCP/IP), so we should implement this protocol for generic data communication. The proposal mentioned that the EoT device should have a MQTT server (i.e. broker).

The result of this task is a library called WifiFunctions, which is an abstraction layer between the Simplelink Wi-Fi driver and the programmer. The functionality provided, apart from the Simplelink driver functions (check CC3100 programmer's guide at http://www.ti.com/lit/ug/swru368a/swru368a.pdf for more information), is as follows:

- Generation of access point.
- Connection to existing access points.
- Scanning of the Wi-Fi spectrum to find the less saturated channel.
- Profile management for saving a previously generated access point, and reusing it when the device is restarted.
- Ping.
- Change own MAC address
- Set Wi-Fi signal intensity and power policy

7.1.5. Vision sensors

The EoT wearable device with the form factor is equipped with a few different cameras to support different purposes and applications. It ranges from a very low

[1] The original proposal is on pages 119-236 of the Grant Agreement pdf document

power and low resolution serial-data camera to a MIPI 1080P high resolution camera. In this section we will review these options.

7.1.5.1. NanEye camera

The NanEye sensor (from Awaiba, Portugal), shown in Figure 6-10, which is an extremely small CMOS image sensor with an integrated lens, is fully self-timed so that once it is powered on it continually transmits image data in rolling shutter mode. Sensor properties including framerate, analogue gain and exposure can be configured by external logic. This sensor was originally designed for medical endoscopy applications natively. Illumination for the sensor is provided by an accompanying light source. With a total volume of 1.7 mm3, the NanEye provides an extremely small, yet fully integrated, imaging solution, which is capable of capturing 250x250 pixel images. This camera consumes less than 5mW at 60 frames per second (fps). The custom lens bonded to the sensor is F2.8 with a 120-degree field of view. Owing to its design as an endoscopic camera, the depth of field is between 5.0 and 35.0 mm. This extremely close focus may present some challenges for the EoT use cases where scene depths are typically much larger (up to room scale). NanEye frame data can be transferred up to 2m over the attached 4 wire LVDS cable.

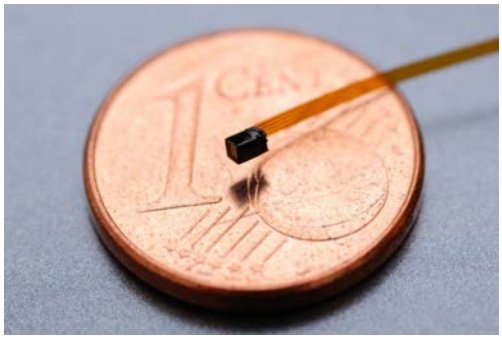


Figure 6-10: NanEye 2D image sensor.

The NanEye is supplied with a DC voltage between 1.8V and 2.4V. Varying the voltage within this range varies the frame rate of the sensor from 40 to 60 frames per second. When supplied with a nominal 2.1V, the sensor consumes 4.2mW. Thanks to this low power consumption, EoT applications can potentially use the NanEye as an 'always on' sensor. As Figure 6-11 shows, the NanEye sensor is bonded to a 4 wire interface, consisting of supply voltage, ground and two serial LVDS data signals.

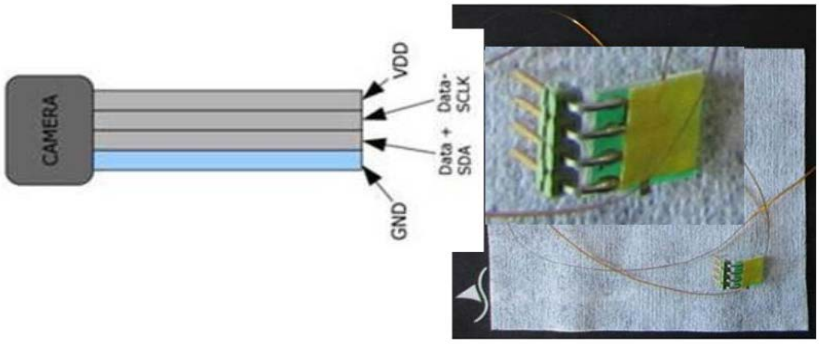


Figure 6-11: NanEye physical interface.

The Movidius Myriad2 processor is configured to receive the NanEye image data over a parallel CIF (Camera Interface) interface. Hence the serial pixel data from NanEye must be decoded and de-serialised before transmission to the Myriad2. Two modes are possible for interfacing the NanEye to the Myriad via the FPGA, Mode A: direct mode; and Mode B: through a signal translator and a comparator. Mode B has been the native option of Awaiba, while Mode A has been the desirable option for EoT due to the lower component count. Since Mode A satisfies EoT requirements, this mode is used in EoT form factor device. Regardless of the mode, the LVDS to CIF conversion is handled with a Lattice MachXO3 FPGA. For the form factor device, a small and low power member of the Mach family, i.e., the LCMXO3L-2100E is used. The FPGA also decodes the frame breaks and transmits the appropriate vertical and horizontal timing signals (VSYNC and HSYNC) to the Myriad, as well as the pixel clock (PCLK). Figure 6-12 shows a block diagram of this chosen interface.

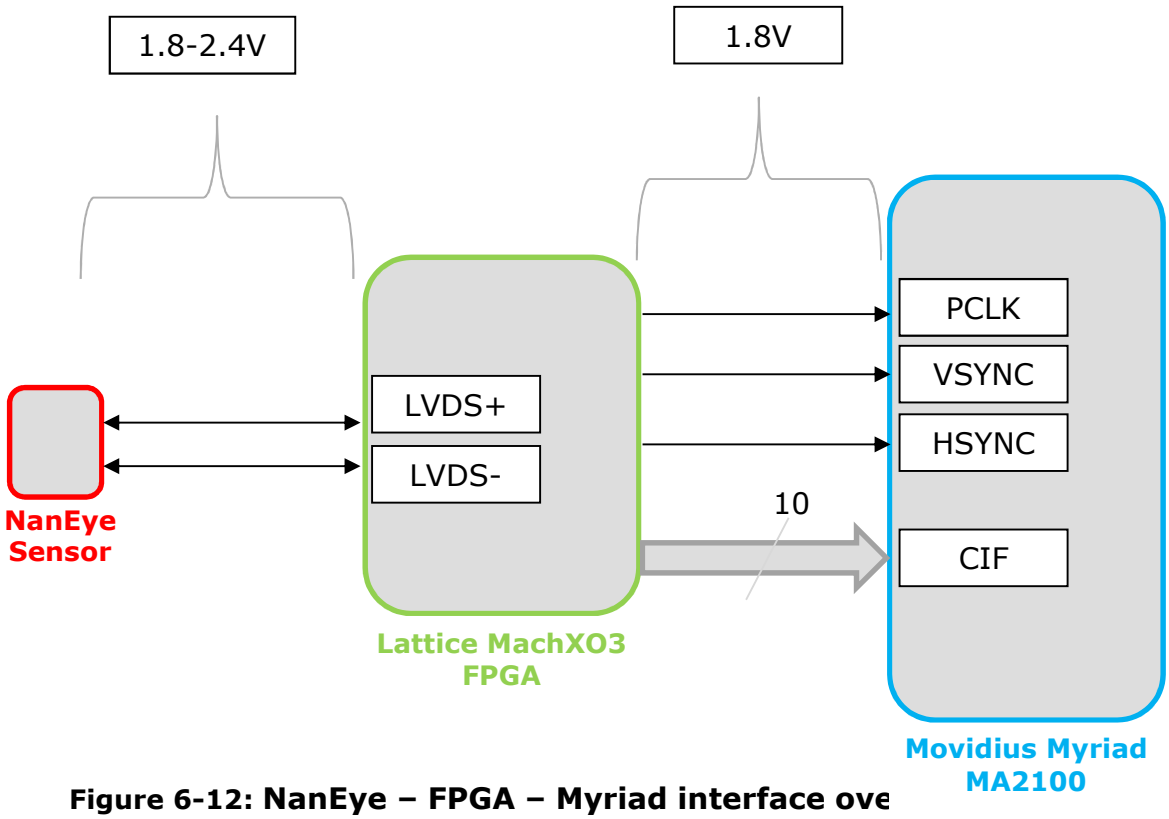


Figure 6-12: NanEye – FPGA – Myriad interface ove

Example NanEye Images

Figure 6-13 shows sample images captured with the NanEye sensor in indoor and outdoor environments. These images have been processed through Awaiba's standard image processing pipeline, which includes debayering, gamma correction and colour correction.

Figure 6-13: Sample debayered images from NanEye sensor (after basic image processing).

7.1.5.2. Himax HM01B0 ultra low power CIS

The HM01B0 is an Ultra-Low Power Image Sensor (ULPIS) that enables the integration of an "Always On" camera for computer vision applications. The unique architecture of the sensor enables the sensor to consume very low power of <4mW at QVGA 60FPS, <2mW at QVGA 30FPS, and <700µW at QQVGA 30FPS.

The HM01B0 contains 320×320-pixel resolution and supports 320×240 window mode which can be readout at a maximum frame rate of 60FPS, and a 2×2 monochrome binning mode with a maximum, frame rate of 120FPS. The video data is transferred over a configurable 1-bit, 4-bit, or 8-bit interface with support for frame and line synchronization. The sensor integrates black level calibration circuit, automatic exposure and gain control loop, self-oscillator and motion detection circuit with interrupt output to reduce host computation and commands to the sensor to optimise the system power consumption.

The sensor is available in a Chip Scale Package (CSP) or bare die and measures less than 5 mm^2. The sensor supports single, dual or triple power supply configuration and requires only three passive components enabling a highly compact camera module design for applications such as IoT, wearable, smart building, tablets, and slim notebooks. Figure 6-14 presents the HM1B0 features.

Sensor	Parameters
Active Pixel Array	320 x 320
Pixel Size	3.6 µm x 3.6 µm
Full Image Area	1152 µm x 1152 µm
Diagonal (Optical Format)	1.63 mm (1/11")
Color Filter Array	Monochrome and Bayer
Scan Mode	Progressive
Shutter Type	Electronic Rolling Shutter
Frame Rate MAX	48 fps @ 320 x 320
	60 fps @ 320 x 240 (QVGA)
S/N Ratio MAX	TBD
Sensitivity	TBD mV / Lux-sec @ 530nm
	TBD mV / (uW-cm^{-2} sec) @ 820nm
CRA (maximum)	30°

General		Value	
Supply Voltage	Analog	2.8 V	
	Digital	1.5V (Internal LDO: 1.5V – 2.8V)	
	I/O	1.5 – 2.8V	
Input Reference Clock		3 – 50 MHz	
Serial Interface (I2C)		2-wire, 400 KHz max.	
Video Data Interface		1b, 4b, 8b with frame / line SYNC	
Output Clock Rate MAX		50 MHz for 1bit	
		25 MHz for 4bit	
		6.25 MHz for 8bit	
Est. Power Consumption (include IO with 5pF load)		QVGA 60FPS (Typical)	<4 mW
		QVGA 30FPS (Typical)	<2 mW
		QQVGA 30FPS (Typical)	670 µW
		Standby	TBD µW

Figure 6-14: Himax HM01B0 sensor features.

Figure 6-15 and Figure 6-16 show the HM01B0 block diagram and raw image sample, respectively.

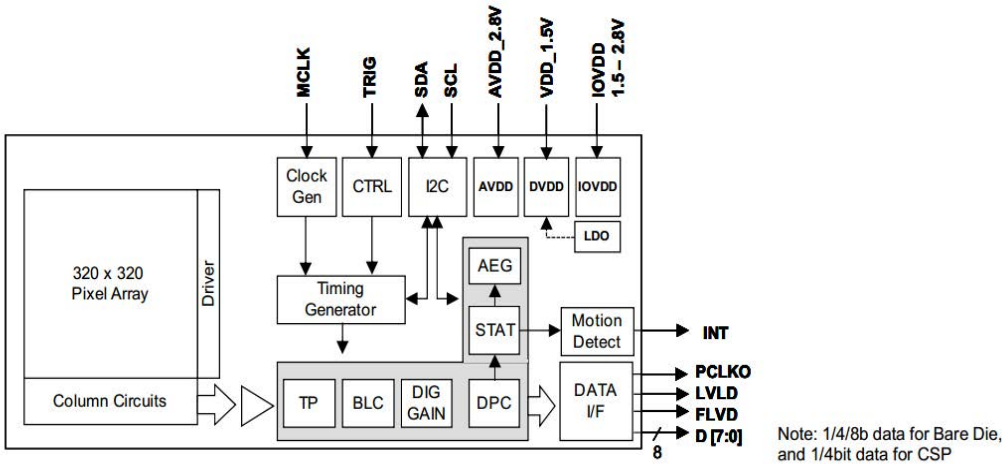


Figure 6-15: HM01B0 block diagram.

Figure 6-16: Himax HM01B0 raw image sample.

7.1.5.3. Secondary high resolution camera:

The EoT wearable device with form-factor board is supported by a higher resolution secondary camera, which is on a daughter-card and is connected to the board through an LSHM connector. This is a Sony IMX208 sensor which communicates with Myriad2 using the MIPI protocol. This camera is not favoured as the primary sensor of EoT wearable device due to its higher power consumption. However, it provides a mean for acquiring the higher 1080P resolution images in case the application needs to capture and/or process more details. Figure 6-17 shows this camera on a daughter-card plugged into the EoT DevBoard through an LSHM connector.

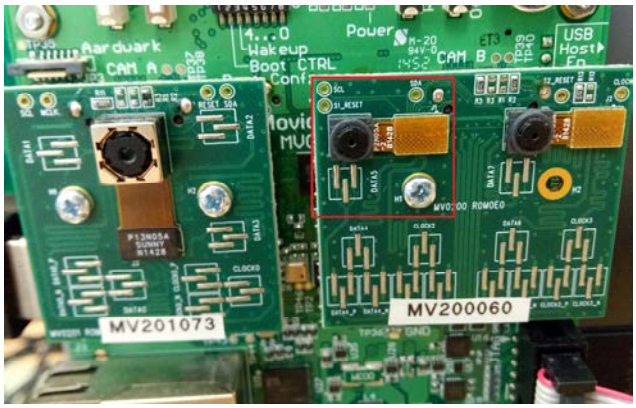


Figure 6-17: MIPI IMX208 camera used for EoT DevBoard.

The EoT DevBoard supported two of these sensors on the camera daughter-card, which allowed doing stereo vision. The EoT device with the form factor board supports one IMX208 sensor along with two Himax HM01B0. It is intended to provide one of the HM01B0 sensors to be pluggable using a connector and used through a 30 cm cable for applications that need this functionality.

7.1.5.4. Camera interface

To provide an easy-to-use interface to connect to the camera and retrieve frames, a camera module has been developed on top of the more complex MDK camera driver (CamGeneric module). This module can be used with any camera in EoT device with only minor changes, yet retaining the same functionality with all cameras. The camera to use is selected with, say, a parameter flag in the code at compile time. Using CamGeneric, the camera should be used according to the following scenario:

In this case, the camera cannot be started and stopped more than one time. However, its standby status can be used to simulate this behaviour and save power. There are two standby configurations:

- HOT STANDBY: the sensor is deactivated but still configured. This standby type is mostly used to save processor time by suspending the interrupts and is fast to recover from (activation last less than 0.5 milliseconds).
- COLD STANDBY: Wakeup out of this state implies full sensor reconfiguration. The wake up duration may last tens of milliseconds.

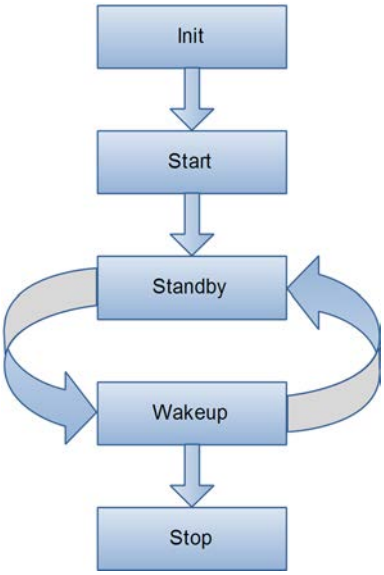


Figure 6-18: Camera execution diagram.

The EoT Camera module supports the HOT STANDBY option. In computer vision applications, the camera should be active only when needed.

The camera interface provides frames in a simple format:

```
typedef struct frameElements
{
     frameSpec spec;
     unsigned char* p1;  // Pointer to first image plane
     unsigned char* p2;  // Pointer to second image plane
     unsigned char* p3;  // Pointer to third image
} frameBuffer;
```

Where spec defines the type of frame (height, width, …). These structures are defined in file swcFrameTypes.h.

Since JPEG is one of the most used image compression standards, JPEG compression support has been added to this module. The Control Mode application (i.e. Pulga) and the RTSP streaming applications send the JPEG-compressed image obtained from the camera.

7.1.6. Power management Unit (PMU)

Power management concerns the supply and control of all electrical power to the form factor board components. The power supply rails must meet the tight specifications of the Myriad2 and other sensitive components, supply switchable voltages for certain applications, and meet specified power-up and power-down timing thresholds. Owing to the wearable nature of the EoT form factor board, power management must maximise the efficiency of power regulation in the minimum board area.

Due to the silicon structure of MA2150 Myriad2 VPU, it must be powered up in a predefined sequence. Within the SoC are two dies - the MA2150 silicon plus a stacked DRAM memory die. These dies have distinctive power requirements that must be met in order to ensure correct SoC operation. Overall the MA2150 has 18 independent power islands that allow fine-grained power management, and these

require multiple supply voltages with separate current draw characteristics so that the islands can be independently powered up and down.

Table 6-1: Power rail requirements for MA2150.

Sequence Stage	Rails Powered	Purpose	Start Time
S0	USB_VDD330	USB Phy High Voltage Analog Supply	T0
	MIPI_VDD	MIPI Analog Supply	
	VDDIO	I/O Supply	
	PLL_AVDD	PLL Analog Supply	
	DRAM_MVDDA	Myriad DDR PLL Analog Supply	
	VDDCR, VDDCV	Core Retention Supply	
	USB_VP_VDD	USB Phy Low Voltage Analog Supply	
	VDDIO_B3.3	IO Supply B Voltage Range	
S1	DRAM_VDD1	DRAM Die Core Power 1	T1
S2	DRAM_VDD2	DRAM Die Core Power 2	T2
S3	DRAM_VDDQ	DRAM I/O Buffer Power	T3
S4	DRAM_MVDDQ	Myriad DDR I/O Supply	T4
Complete			T5

The list of individual power rails for the MA2150 are provided in Table 6-1. They are logically grouped into sequence stages from S0 to S4, where all the rails in each stage power up together. Requirements for the stage sequence timing are shown in Table 6-2. Although valid power-up can be achieved in less than 5 stages, depending on the required Myriad functionality and the connection of peripheral components, specifying power management requirements for the full 5 stage start-up provides maximum application flexibility. The mandatory power sequencing concerns the DRAM die supplies.

Table 6-2: Power supply timing requirements for MA2150.

Timing Requirements		Notes
1	T5-T0<=20ms	Not mandatory but considered good practice
2	T5-T4>=1ms	Suggested but not mandatory. However, voltages in the previous stage should have reached their nominal values before starting the next stage
	T4-T3>=1ms	
	T3-T2>=1ms	
	T2-T1>=1ms	
3	T5-T2<=20ms	Mandatory (DRAM_VDD1, DRAM_VDD2, DRAM_VDDQ rise times from 300mV to start of operating range < 20ms)
4	All rise times > 10us	Mandatory

The voltage and current specification for the MA2150 supply rails are presented in Table 6-3**¡Error! No se encuentra el origen de la referencia.**. Current draw is dependent on processing load, but should not exceed the specified values. Power rails are individually switchable to enable power saving by powering down power islands. VDDIO_B3.3 is additionally switchable between 1.8V and 3.3V to natively meet the two different speed standards for SD card IO.

Table 6-3: Power supply definition for MA2150.

Power Rail	Purpose	Nominal Voltage (V)	Maximum Current (mA)
USB_VDD330	USB Phy High Voltage Analog Supply	3.3	80
MIPI_VDD	MIPI Analog Supply	1.8	60
VDDIO	I/O Supply	1.8	250
PLL_AVDD	PLL Analog Supply	1.8	10
DRAM_MVDDA	Myriad DDR PLL Analog Supply	1.8	80
VDDCR, VDDCV	Core Retention Supply	0.9	2600
USB_VP_VDD	USB Phy Low Voltage Analog Supply	0.9	66
VDDIO_B3.3	IO Supply B Voltage Range	1.8/3.3 switchable	
DRAM_VDD1	DRAM Die Core Power 1	1.8	25
DRAM_VDD2	DRAM Die Core Power 2	1.2	220
DRAM_VDDQ	DRAM I/O Buffer Power	1.2	25
DRAM_MVDDQ	Myriad DDR I/O Supply	1.2	300

The EoT form factor board is a wearable/portable device and in normal operation will be battery powered with a 3.7V Lithium-ion Polymer (Li-Po) battery. When tethered, such as during code development, testing and validation, the board should be powered from a non-battery source. Two options are available for tethered powering: (1) a standard mains powered step-down transformer connected to a dedicated on-board power jack; (2) USB cable connected to a micro-USB on-board port. The USB option was chosen for tethered supply to the EoT form factor board. Battery recharging via this micro-USB port is a 'nice-to-have' feature, but is not a requirement for the form factor board. The acceptable alternative to on-board charging would be to disconnect the discharged battery from the board and connect it to a dedicated charger.

The previous EoT DevBoard had a WM8325 PMIC from Wolfson. The RC5T619 Power Management Unit (PMU) from Ricoh Electronic Devices Company is used for the EoT form factor board due its strength in powering via USB, the 'nice to have' on-board battery recharging feature, and the ability to switch between USB and battery. In volume the RC5T619 is also very competitively priced. Figure 6-1 shows the PMU functionality that is of primary relevance to the EoT form factor board. Also shown are the range of voltage and current outputs that each DCDC and LDO can provide. The DCDC and LDO outputs can be allocated across 15 sequence stages, with 0.5/2ms separation between stages. Output voltages are configurable in 12.5mV steps for the DCDCs, and in 25mV steps for the LDOs.

The RC5T619 is targeted at wearable and IoT applications, and its low consumption current (0.5mA in typical operating mode) is ideally suited to the form factor board. The RC5T619 has OTP functionality only and is factory programmed before shipment. Once the PMU has been programmed by OTP, changes can be made via I2C from the MA2150. The size of the bounding box for the minimal-boardspace layout, provided by Ricoh, is 18.6mm x 25mm. Some example drivers for the various RC5T619 functions have also been provided by Ricoh. Figure 6-20 shows the input power supply to the PMU via USB and/or battery.

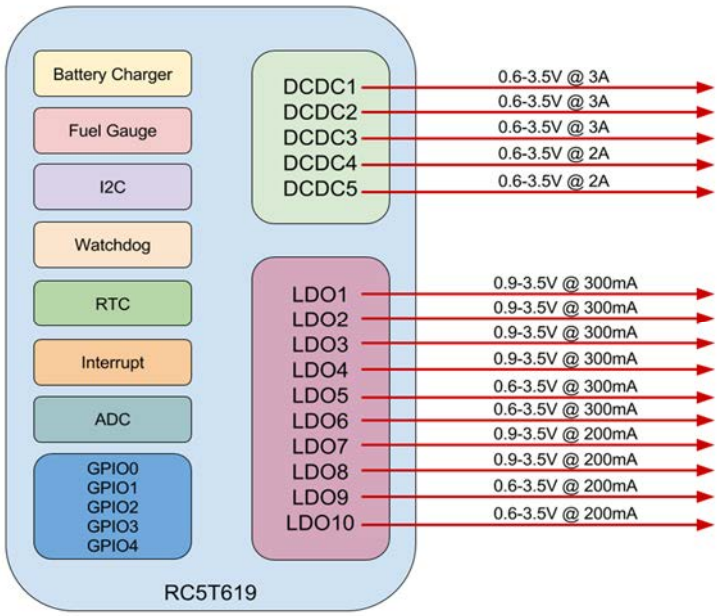


Figure 6-19: RC5T619 PMU functional outline.

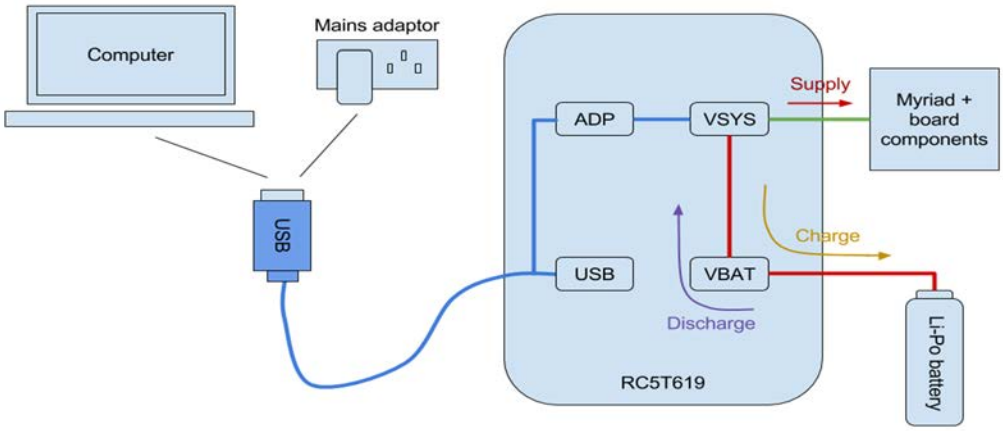


Figure 6-20: PMU power paths.

7.1.7. Motor control

The Motor Control module provides the EoT board with a means of communicating with a wide variety of devices such as robots, drones, actuators and sensors. This means that it is possible to control small robot cars and flying drones; open and close doors as required; monitor devices such as fridges, vending machines; or control systems like air conditioning and lighting which might not have access to internet or wireless connectivity.

Figure 6-21: Cherokey 4WD from DFRobot.

The Motor Control module (a C/C++ library) encapsulates the hardware details of the communication into an easy-to-use API, which could be extended to support multiple devices. As the proof of concept for this application, the robot car Cherokey[2] 4WD from DFRobot[3] was selected as it is low-cost and has a robust aluminium frame. Additionally, an Android App was developed to allow the remote control of a ground vehicle via Wi- Fi. The micro-python version of this API also has been developed for the EoT device. The current implementation of the Motion Control API provides the following functions for controlling ground vehicles:

- Move forward,
- Move backward,
- Tank-turn left
- Tank-turn right
- Stop

The Cherokey 4WD is controlled by four signals in the range of 0-5V, which is compatible with the pins in EoT Motor Control Header. The hardware connection between the Cherokey 4WD and EoT board is summarized in Table 6-4. The EoT form factor board has been designed for maximum flexibility when interfacing with robots and external sensors. All control signals are level shifted up to an externally supplied voltage. By supplying the device's IO voltage to the EoT board, no additional components are required in order to communicate with and control devices with IO voltages anywhere in the range 1.8V to 5V. Level shifting is applied on-board to all communication protocols (I2C, SPI, UART). Additionally, all general purpose IO signals are bi-directionally level-shifted.

Table 6-4: Connection between the EoT DevBoard and the Cherokey 4WD

EoT Motor Control Header Pin	Cherokey 4WD Pin
3: PWM0	D5:M1_PWM
4: PWM1	D7:M2_PWM
5: DIR0	D4:M1_EN
6: DIR1	D6:M2_EN
7: GND	GND

[2] http://goo.gl/7Gxi6n
[3] http://www.dfrobot.com

7.1.8. Audio input & output

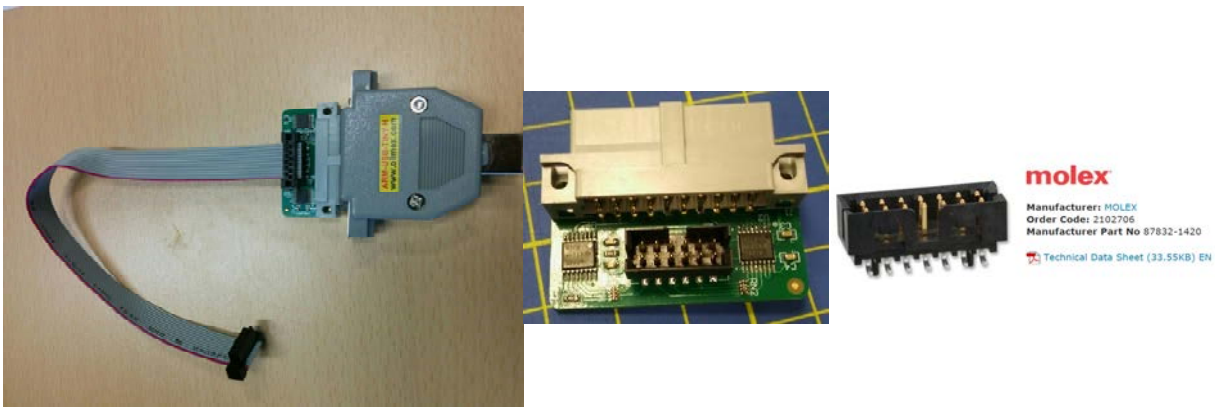
The audio module provides access to the audio chip for playback and recording of audio signals. Furthermore, encoding and decoding of the Opus[4] audio format is supported (a codec is needed for audio streaming). Audio data can be read from and written to files in the OGG container format. The audio chip is configured by this module through the I2C interface and audio data is transmitted through the I2S interface.

7.1.9. Device connectivity

EoT device with the form factor board is accessible in different ways as will be listed and explained in this section.

7.1.9.1. JTAG debugging connector

For the sake of debugging, the EoT device would be accessible through the JTAG debugging connector. The EoT device is connected to the USB port of a PC though the MV0218 JTAG Level Shifter and an Olimex connector (see Figure 6-22). We use the low profile JTAG connector MOLEX 87832-1220 for EoT device.



a b c

Figure 6-22: MV0218 JTAG and Olimex connector.

7.1.9.2. UART

To provide the serial asynchronous communication with the Myriad2, the EoT device with form factor board has a bidirectional level-shifted UART I/O.

7.1.9.3. USB connector

The Micro USB 3.0 is used as another input/output port for the EoT device. This port is used for data exchange as well as supplying the board with power. Battery charging is another task that is available through the USB port of the form factor board.

7.1.9.4. SD Card

Owing to definition of the device, a MicroSD card connector has been added to the board to provide storage of data on the device. The SD card management is

4 Opus Interactive Audio Codec: https://www.opus-codec.org/

handled using a module that contains functions to provide access to files and directories on the SD card. It supports file level encryption (only file contents, not metadata) through the use of the EoT library "Crypto". Furthermore, it can also be used to mount and unmount the SD card. The module uses FAT32 as file system and builds on top of the file system functionality provided by RTEMS.

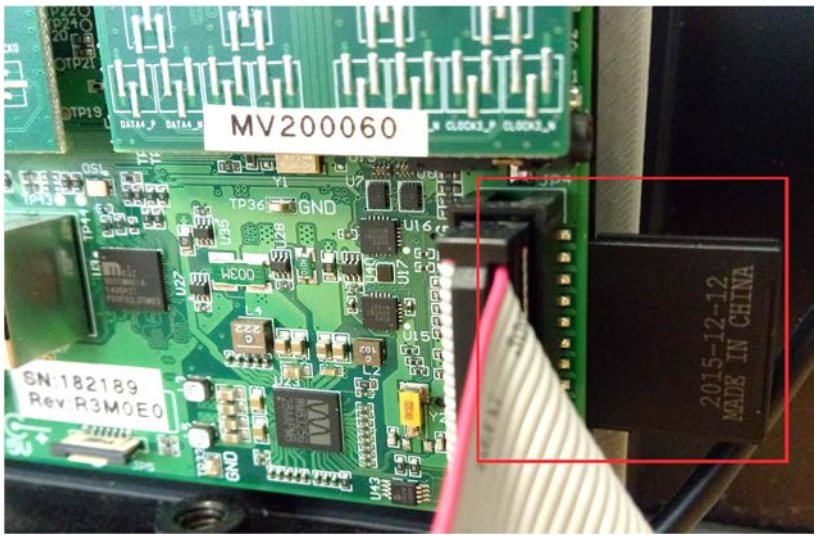


Figure 6-23: SD card slot on the DevBoard.

The DevBoard version of EoT board has an EEPROM to support writing and reading the board revision. To save board space and components in the EoT device with the form factor board, the EEPROM has been deleted and the board revision info is written and read from the SD card instead.

7.1.9.5. Optical audio jack

Beside the standard 3.5mm audio jack which is available on the board, an extra audio connection possibility also has been added to the EoT device with the form factor board. Owing to higher baud-rate of light transmission and also noise free communication over the optical audio connection, the optical audio jack with the related functionality to convert the audio signal into the appropriate format has been added to the device. The standard audio jack, the optical audio jack, and the battery socket and the microphone are connected to the board using flex-cables for the sake of space saving.

7.1.10. Unused GPIOs and Break-off sections

To provide more opportunity for developers to implement their ideas, we decided to expose the unused GPIO pins on the edge of the board using 0.1" headers. It will take two sides of the board approximately (see Figure 7-1).

Since the FfBoard is a wearable device that is supplied by battery, it is desirable to reduce the size and weight (in case of being used for drones) of the board as much as possible. Therefore, we planned to push the optional components to the edge of the board using a snap-off scenario. In this way, the user can break those parts and make the board smaller and lighter. The test points are also located on the break-off area to provide debugging and testing opportunity for the developers. Figure 7-1 shows the EoT device with form factor board modular block diagram along with the break-off sections.

A block diagram of the complete system is shown in Figure 6-24.

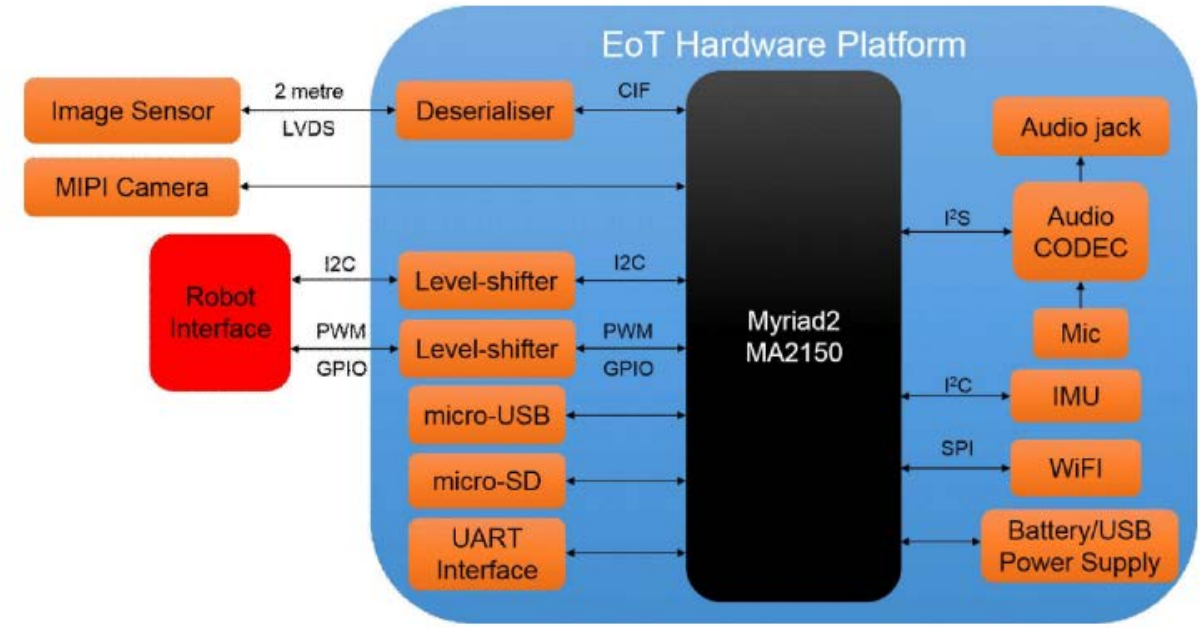


Figure 6-24: EoT Hardware Platform.

EoT Form Factor Board Optimised Software

7.2.1. Fathom Deep-Learning Framework

Many large companies have invested heavily in machine intelligence for vision and other applications over the past five years. To date these applications have been largely confined to the cloud. Given the difficulties in scaling vision based solutions which include power dissipation, latency, continuity of service, bandwidth and privacy, there is huge interest in migrating such applications in whole or in part to the network edge.

In order to address these needs Movidius has developed a framework, called Fathom, for implementing CNNs of various configurations at ultra-low power targeting the Myriad2 VPU. The Fathom framework accepts xml representations of trained networks from Caffe or TensorFlow as shown in . Fathom parses these representations and optimally translates them to run on the Myriad2 VPU architecture. For complex networks such as GoogleNet, Fathom enables performance at a nominal 15 inferences/sec with fp16 precision on Myriad2 MA2450 (512MB stacked LPDDR3 die in package).

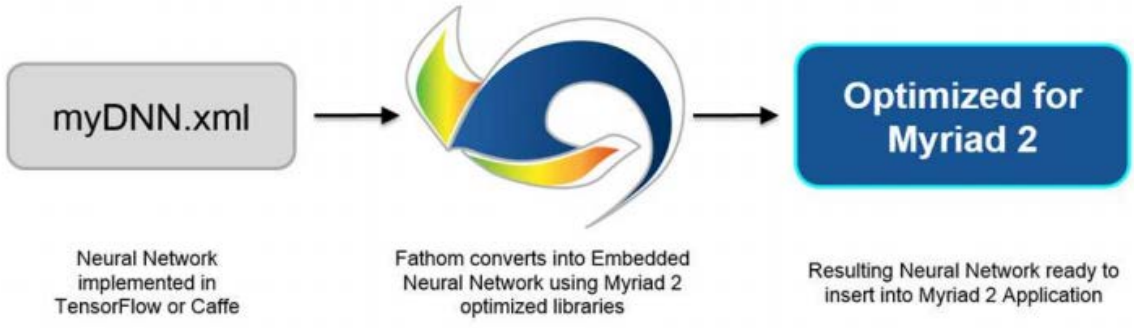


Figure 6-25: Fathom Deep-Learning Framework.

The mVTensor library is built on top of the mvMatMul library, and MvTensor library provides highly efficient 3D/4D convolution with an initial focus on strided small convolutions required by GoogleNet. The basic concepts and scheduler used in mvMatMul are described in "The Movidius Myriad Architecture's Potential for Scientific Computing", the published paper in IEEE Micro[5].

The Fathom framework builds on top of software library (MvTensor) and hardware acceleration support in present and future Myriad devices as shown in

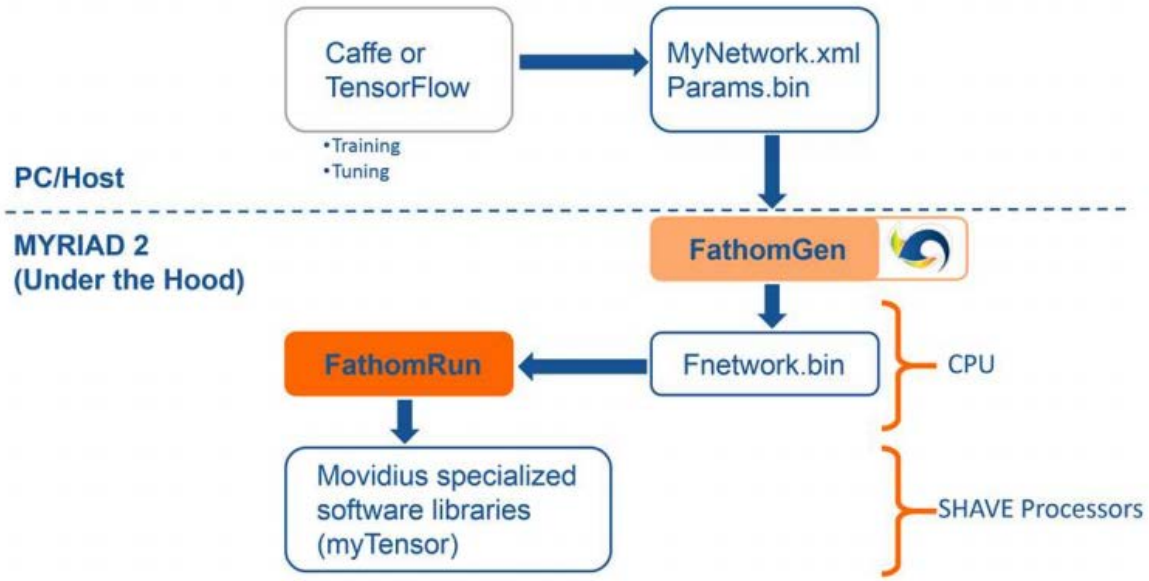


Figure 6-26: Fathom Framework Details.

7.2.2. Computer Vision Libraries

While libraries such as OpenCV6 and libccv7 have been ported to the Myriad2 platform as part of the EoT framework they have not been performance optimised for the SHAVEs. For high performance and low-power computer vision Movidius provides a proprietary library called MvCV which takes advantage of the various features of the Myriad architecture to achieve maximum performance at minimum power. One of the key optimisations is to operate on stripes or tiles from a frame

[5] M. H. Ionica and D. Gregg, "The Movidius Myriad Architecture's Potential for Scientific Computing," in *IEEE Micro*, vol. 35, no. 1, pp. 6 14, Jan.-Feb. 2015

[6] http://opencv.org/

[7] http://libccv.org/

rather than going round trip to DRAM each time which greatly reduces power and maximizes performance.

The MvCv library has been used across dozens of customer projects and contains hundreds of commonly used CV functions including: a high performance multi-frame point tracker called vTrack, Visual Odometry, HoG, Kalman/ROI, h264 video-codec, SGBM, BLIS, JPEG codec, Image Warp, RANSAC, FREAK and various linear algebra solvers.

7.2.3. Pulga MQTT Broker

Typical Internet communication protocols are not appropriate for an IoT context. HTTP, for example, is text oriented, which means that more bits are needed to transfer the same information. EoT communication with the outside world is based on MQTT[8], an open lightweight publish/subscribe protocol based on TCP/IP. Devices that support this protocol can open a connection, maintaining it using very little power while receiving commands with as little as 2 bytes of overhead. While HTTPS is slightly more efficient in terms of establishing a connection, MQTT is much more efficient during transmission.

With MQTT, the classic approach is that an embedded client connects to an MQTT server (broker) in the cloud. In this scenario the server has to be leased by the user, or else it has to be installed on a locally-managed server. In EoT, the device actually implements a broker (called Pulga), which means that an external server is not needed (although it can be used). This approach allows other EoT devices to subscribe to another EoT. Furthermore, an external device can be used to send/receive configuration commands to the EoT board using MQTT messages. This approach has been followed in EoT, which exposes a number of basic configuration commands to external devices (PC, tablet or smartphone). shows the client application running on a PC.

[8] http://mqtt.org/

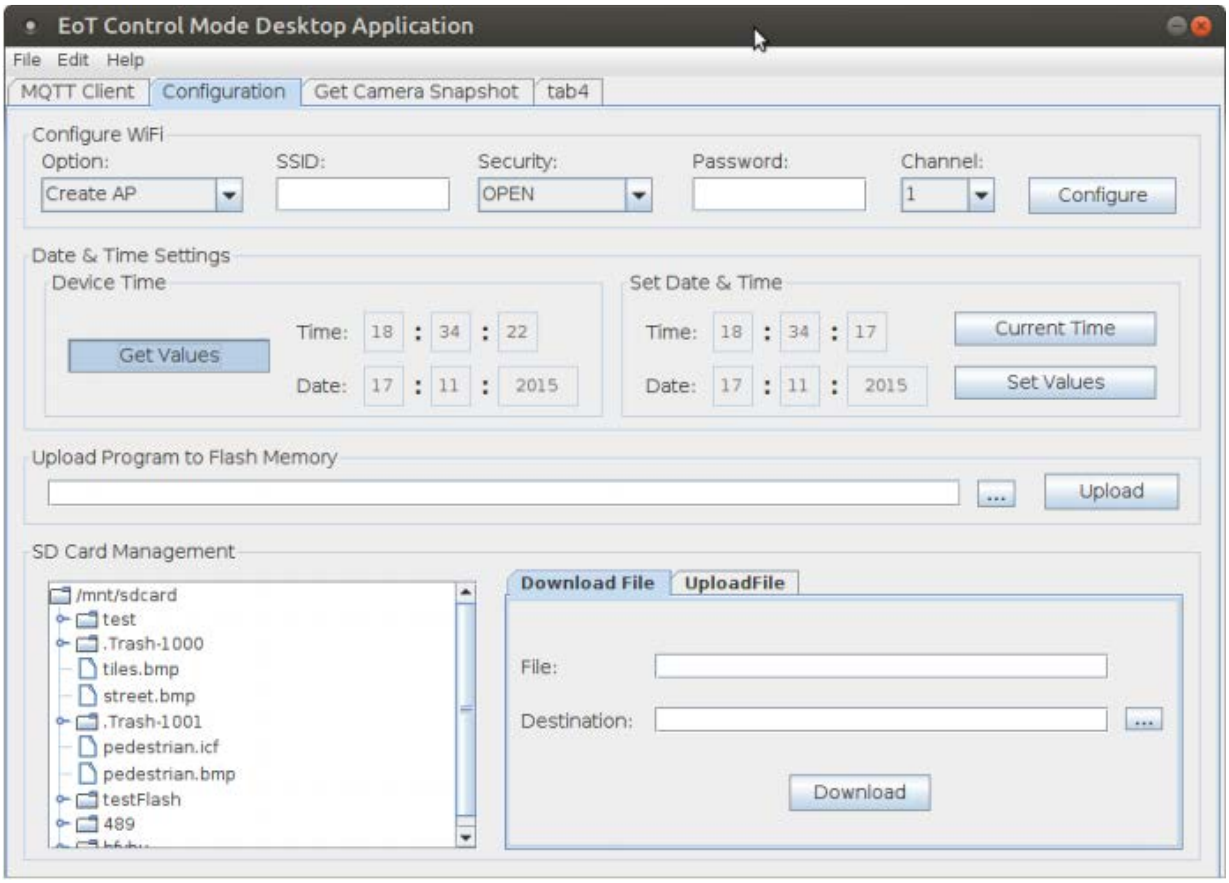


Figure 6-27: Pulga MQTT client application running on a PC.

7.2.4. Micropython

The Python programming language's flexibility and ease-of-use have made it wildly popular in academia and in general in many realms where speed of development and flexibility is more important than performance. Python is an interpreted language, which means that it is not in principle a good fit for embedded systems. In the past, a number of attempts have been made at porting it to embedded platforms. MicroPython is currently the most successful port[9]. It is a C language port of the Python 3 language. The EoT board supports MicroPython. A REPL system is already available on top of the MQTT communication protocol. This allows sending of instructions and receiving responses remotely, from a PC or tablet, see Fig. 0. Work is currently underway to extend the language to use the EoT hardware capabilities.

[9] https://micropython.org/

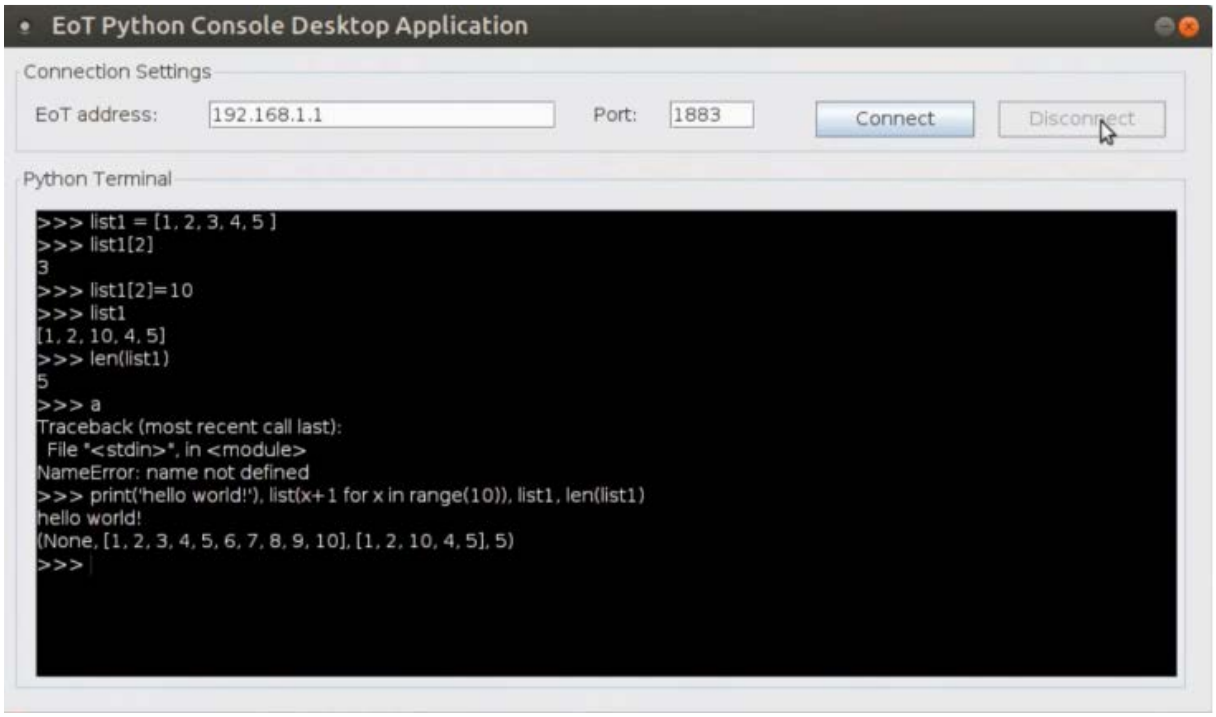


Figure 6-28: EoT MicroPython remote terminal.

8. EOT FORM FACTOR BOARD SPECS

The board vendor selection was started by quoting from a number of different companies with different expertise. After reviewing the quotes, the Italian company DPControl was selected as the board vendor for the project due to their superb experience in form-factor design as well as the competitive price they offered. Owing to the significant changes from EoT DevBoard (the non-form-factor board) to EoT form-factor board, and due to the nature of the form-factor design it was planned to have two stages of the design and manufacturing process in order to minimize risk and expenses. On this basis, it was planned to manufacture the Validation version of the design with two more layers to expose the test points to the PCB top and bottom layer, firstly. Then, the final form-factor board is refined using the results of testing the validation board.

The overall work package foresees the design, manufacturing, assembly, and test of a 5 validation form-factor as well as 40 final form-factor boards for the EoT project. The form-factor PCB has been designed based on the EoT DevBoard PCB in Altium, while it complies the changes according to spec as well as the quote. As shown in Fig.Figure 7-2, the form-factor PCB should include the following features and specifications:

- **Shape**: desired 1.5x3 cm, to be confirmed after preliminary checks (min. 1.5 x 3 cm – max 2.0x4.5 cm).
- **Validation board:** with more layers and with test points for debugging.
- **Form-factor board**: based on the results of testing the validation boards and its layout may or may not be same as the validation board.
- **Principal active/passive components/subsystems**:
    - VPU: MA2150 SoC.
    - FPGA: Lattice Mach XO3 for NanEye deserialization; iCE40 for Himax HM01B0 deserialization
    - Wi-Fi: SPI Wi-Fi I/F (canned CC3100, the CC3100MOD SimpleLink Certified Wi-Fi Network Processor Internet-of-Things Module Solution for MCU Applications.
    - Motor control.
    - BMX-055 IMU with I2C interface.
    - SPI Flash for boot.
    - Clock generation.
    - Power Management IC + USB VCC.
    - USB2.0 Micro port.
    - JTAG connector (low profile).
    - MicroSD socket.
    - TI TLV320AIC3204 CODEC I2S interface, connected to an on-board microphone and to a headphone jack.
    - Connectors:
        - LSHM MIPI camera.

- NanEye camera (4 pins).
- FPGA programmer (8 pins).
- Motor control header.
- Unused GPIO pins.

- **SMT mounting**: top and bottom layer.
- Presence of fine pitch BGA, 0.4mm minimum required.
- **Break-off sections**: sections specified in the modular block diagram of Figure 7-1 could be on break-off section.

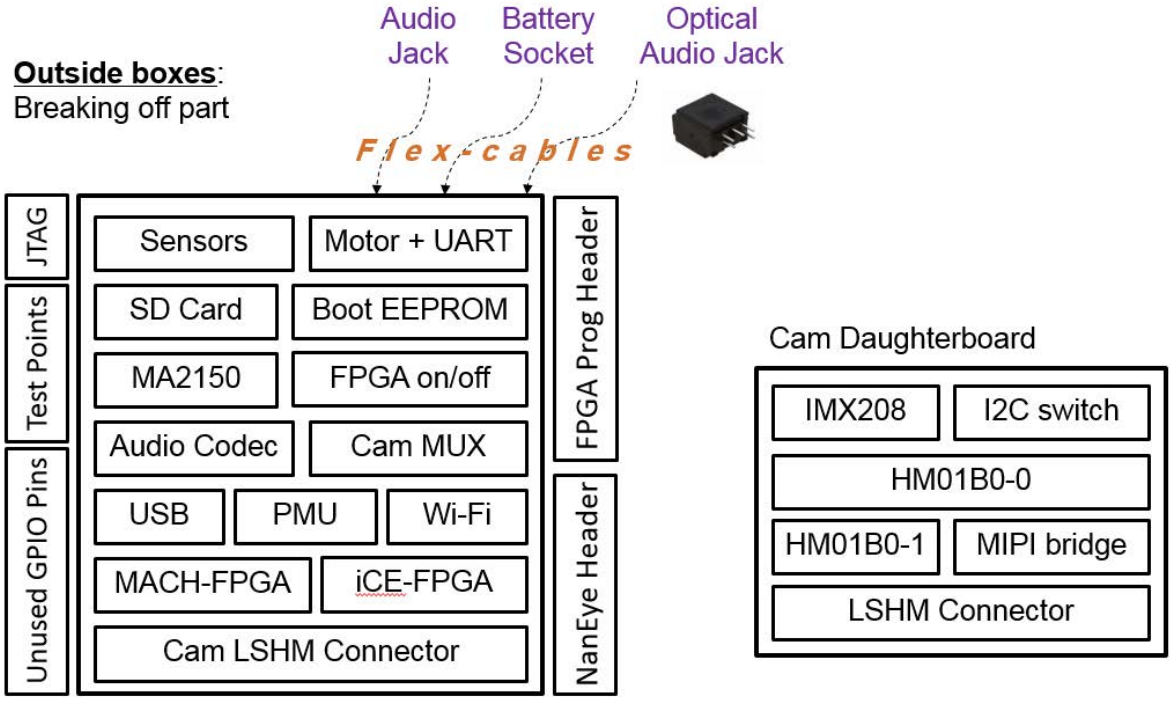


Figure 7-1: EoT FfBoard modular block diagram.

Figure 7-2 shows the specification standard on which the EoT form factor board PCB layout has been developed.

Technology and stack-up	8 layers, Material TG 150
PCB shape	Min. 15 x 30 mm – max 20 x 45 mm
Thickness	1,55mm
Structures outside	>= 250um
Structures inside	>= 192um
Final drill diameter	>= 0,10 mm
Smallest rout tool	<= 1,0mm and >= 0,50mm
Copper thickness	35um outside, 35um inside
Surface finish	Electroless nickel gold (ENIG)
Additional surface	Top+Bottom, hard gold with plating ties
Solder resist	Top+Bottom, color to be defined
Silk screen	Top+Bottom, white
E-test	Yes
UL marking	Yes, standard compliant
Additional documentation	Certificate of Conformity

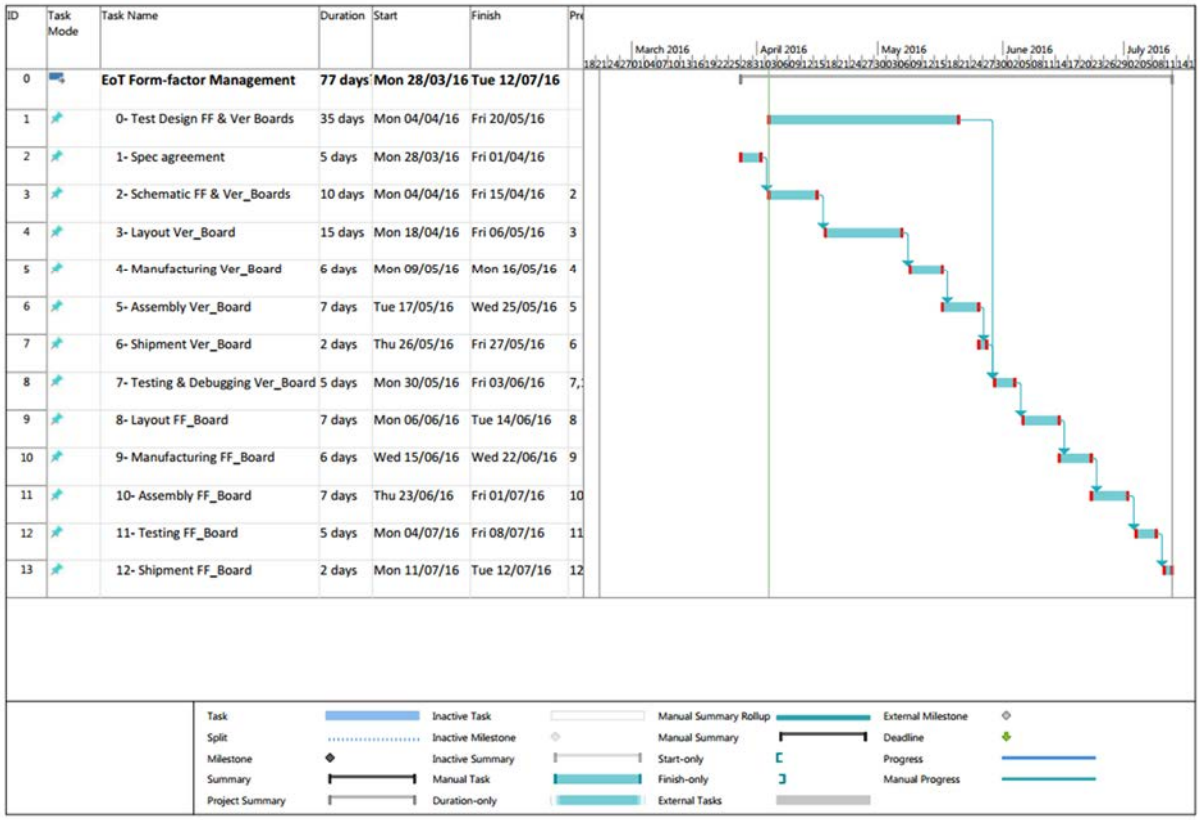
Figure 7-2: PCB layout specification standard.

EoT Form Factor Board Timeline

According to the timeline below, the total term of form-factor board design and manufacturing is going to be 77 working days, commencing on the 28st of March 2016 and terminating on the 12th of July 2016. The term may be extended by mutual agreement between the parties. Table 7-1 shows the project timeline.

Table 7-1: EoT form-factor board tasks/timeline

ID	Task Mode	Task Name	Duration	Start	Finish	Pre
0		**EoT Form-factor Management**	**77 days**	**Mon 28/03/16**	**Tue 12/07/16**	
1		0- Test Design FF & Ver Boards	35 days	Mon 04/04/16	Fri 20/05/16	
2		1- Spec agreement	5 days	Mon 28/03/16	Fri 01/04/16	
3		2- Schematic FF & Ver_Boards	10 days	Mon 04/04/16	Fri 15/04/16	2
4		3- Layout Ver_Board	15 days	Mon 18/04/16	Fri 06/05/16	3
5		4- Manufacturing Ver_Board	6 days	Mon 09/05/16	Mon 16/05/16	4
6		5- Assembly Ver_Board	7 days	Tue 17/05/16	Wed 25/05/16	5
7		6- Shipment Ver_Board	2 days	Thu 26/05/16	Fri 27/05/16	6
8		7- Testing & Debugging Ver_Board	5 days	Mon 30/05/16	Fri 03/06/16	7,
9		8- Layout FF_Board	7 days	Mon 06/06/16	Tue 14/06/16	8
10		9- Manufacturing FF_Board	6 days	Wed 15/06/16	Wed 22/06/16	9
11		10- Assembly FF_Board	7 days	Thu 23/06/16	Fri 01/07/16	10
12		11- Testing FF_Board	5 days	Mon 04/07/16	Fri 08/07/16	11
13		12- Shipment FF_Board	2 days	Mon 11/07/16	Tue 12/07/16	12



At the time of writing, stage 3 of the timeline has been completed. Stage 4- Validation board layout is in progress and it should be finished by the end of July 2016. This means that by the end of August 2016 five Validation boards would be ready for testing, debugging and verification. Immediately after design approval, the changes, if any up to the result of the tests, will be applied to the schematic and layout and then 40 final EoT form-factor boards will be manufactured, assembled and tested.

EoT Form Factor Board GPIOs Arrangement

Due to the HW changes that have happened in EoT form factor board, a GPIO rearrangement has been performed to comply with these changes. TableTable 7-2 lists the new GPIO arrangement for the EoT device with the form factor board.

Table 7-2: EoT form factor board GPIO arrangement.

		EoT Validation Board Mapping	

MA2150 pin	GPIO function	GPIO names	Mode
gpio_0	i2s1_sck	H1_MCLK	1
gpio_1	cam_pclk	NanEye-PCLK	0
gpio_2	cam_vsync	NanEye-VSYNC	0
gpio_3	cam_hsync	NanEye-HSYNC	0
gpio_4	cam_data0	NanEye-D0	0
gpio_5	cam_data1	NanEye-D1	0
gpio_6	cam_data2	NanEye-D2	0
gpio_7	CPU direct control	BMX_055_INT3	7
gpio_8	spi2_mosi	spi2_mosi	3
gpio_9	spi2_miso	spi2_miso	3
gpio_10	spi2_sclk_out	spi2_sclk_out	3
gpio_11	spi2_ss_out_in_0	spi2_ss_0	3
gpio_12	i2c1_scl	i2c1_scl	2
gpio_13	i2c1_sda	i2c1_sda	2
gpio_14	uart_apb_sin	M_UART-RX	1
gpio_15	uart_apb_sout	M_UART-TX	1
gpio_16	SD_HST1_DAT_3	SD_HST1_DAT_3	3
gpio_17	SD_HST1_CLK	SD_HST1_CLK	3
gpio_18	SD_HST1_CMD	SD_HST1_CMD	3
gpio_19	SD_HST1_DAT_0	SD_HST1_DAT_0	3
gpio_20	SD_HST1_DAT_1	SD_HST1_DAT_1	3
gpio_21	SD_HST1_DAT_2	SD_HST1_DAT_2	3
gpio_22	CPU direct control	MOTOR.DIR0	7
gpio_23	CPU direct control	WIFI-IRQ	7
gpio_24	CPU direct control	CDONE	7
gpio_25	CPU direct control	RH_IRQ	7
gpio_26	CPU direct control	PB_1	7
gpio_27	CPU direct control	PB_2	7
gpio_28	I2S0_SCK	I2S0_SCK	3
gpio_29	I2S0_WS	I2S0_WS	3
gpio_30	I2S0_IN_SD0	I2S0_IN_SD0	3
gpio_31	CPU direct control	BMX_055_INT1	7
gpio_32	CPU direct control	BMX_055_INT5	7
gpio_33	CPU direct control	GPIO33	7

gpio_34	I2S0_OUT_SD0	I2S0_OUT_SD0	3
gpio_35	cam_data3	NanEye-D3	2
gpio_36	cam_data4	NanEye-D4	2
gpio_37	cam_data5	NanEye-D5	2
gpio_38	cam_data6	NanEye-D6	2
gpio_39	cam_data7	NanEye-D7	2
gpio_40	cam_data8	NanEye-D8	2
gpio_41	cam_data9	NanEye-D9	2
gpio_42	cam_data10	cam_data10	2
gpio_43	cam_data11	cam_data11	2
gpio_44	CPU direct control	CAM_B_GPIO0	7
gpio_45	SPI0_MOSI	SPI0_MOSI	4
gpio_46	SPI0_MISO	SPI0_MISO	4
gpio_47	i2s2_sck	i2s2_sck	2
gpio_48	i2s2_ws	i2s2_ws	2
gpio_49	i2s2_in_sd0	i2s2_in_sd0	2
gpio_50	i2s2_in_sd1	i2s2_in_sd1	2
gpio_51	I2s2_in_sd2	I2s2_in_sd2	2
gpio_52	CPU direct control	GPIO52/BOOT1	7
gpio_53	CPU direct control	GPIO53/BOOT2	7
gpio_54	spi0_ss_out_in_1	SPI0_SS_1	4
gpio_55	CPU direct control	WIFI-nHIB	7
gpio_56	CPU direct control	CLK_SEL/BOOT3	7
gpio_57	spi0_ss_out_in_2	SPI0_SS_2	4
gpio_58	spi0_sclk_out	SPI0_SCLK_OUT/BOOT4	4
gpio_59	CPU direct control	NanEye/Himax-MUX	7
gpio_60	i2c0_scl	I2C0_SCL	0
gpio_61	i2c0_sda	I2C0_SDA	0
gpio_62	pwm_out_3	MOTOR.PWM0	4
gpio_63	pwm_out_4	MOTOR.PWM1	4
gpio_64	CPU direct control	FPGA-on_off	7
gpio_65	cam_data12	cam_data12	4
gpio_66	cam_data13	cam_data13	4
gpio_67	cam_data14	cam_data14	4
gpio_68	cam_data15	cam_data15	4

gpio_69	CPU direct control	LED1	7
gpio_70	CPU direct control	sd_pwr_ctr	7
gpio_71	CPU direct control	CRESETB	7
gpio_72	CPU direct control	WIFI-RST	7
gpio_73	CPU direct control	CAM_B_GPIO1	7
gpio_74	CPU direct control	GPIO74	7
gpio_75	CPU direct control	H1_INT	7
gpio_76	CPU direct control	H012_TRIG_I	7
gpio_77	spi0_ss_out_in_0	SPI0_SS_0	0
gpio_78	CPU direct control	MOTOR.DIR1	7
gpio_79	i2c2_scl	I2C2A_SCL	2
gpio_80	i2c2_sda	I2C2A_SDA	2
gpio_81	cpr_io_out_clk_1	AUDIO_MCLK/BOOT0	2
gpio_82	CPU direct control	MOTOR.BRAKE0	7
gpio_83	CPU direct control	H02_INT	7
gpio_84	CPU direct control	MOTOR.BRAKE1	7

As mentioned in deliverable D2.5, some of the GPIO pins are exposed to the edge of the board using 0.1” headers to provide more opportunity for developers to implement their ideas. In this way, they will have access to I2S, I2C, supply voltage (3.3, 2.8, and 1.8 volt), GND, and camera data and configuration pins. There are also a few unused GPIOs that can be used up to the user’s need. The pins on the edge take approximately two sides of the board. Table 7-3 lists these pins in a categorized way.

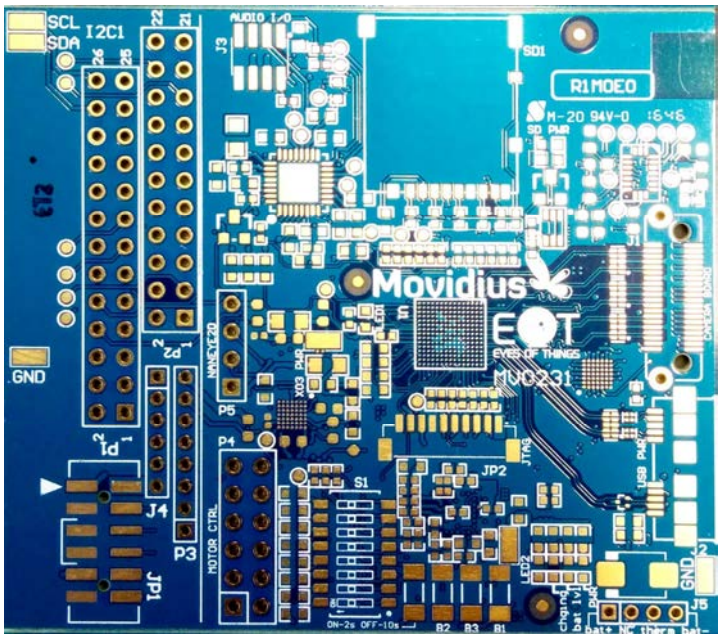
Table 7-3: List of GPIOs on the edge of the board.

ID	GPIO	ID	GPIO
1	3.3VLDO3_7	25	cam_data10
2	GND	26	cam_data11
3	1.8VDC4	27	SPI0_MOSI
4	2.8VLDO11	28	SPI0_MISO
5	GND	29	i2s2_sck
6	GND	30	i2s2_ws
7	GPIO52	31	i2s2_in_sd0
8	GPIO33	32	i2s2_in_sd1
9	NanEye-PCLK	33	I2s2_in_sd2
10	NanEye-VSYNC	34	GPIO53

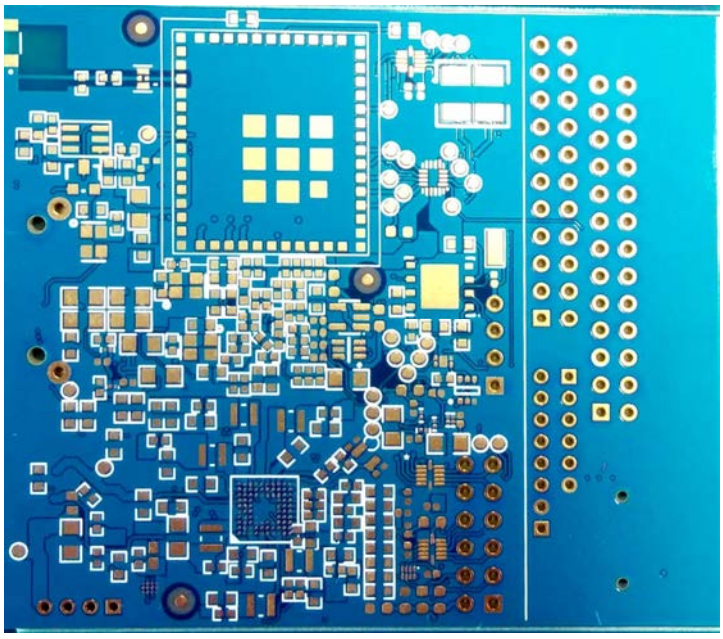
11	NanEye-HSYNC	35	SPI0_SCLK_OUT
12	NanEye-D0	36	cam_data12
13	NanEye-D1	37	cam_data13
14	NanEye-D2	38	cam_data14
15	I2C1_SCL	39	cam_data15
16	I2C1_SDA	40	GPIO33
17	NanEye-D3	41	SPI0_SS_1
18	NanEye-D4	42	H1_HSYNC
19	NanEye-D5	43	H1_VSYNC
20	NanEye-D6	44	H1_PCLK
21	NanEye-D7	45	H1_MCLK
22	NanEye-D8	46	H1_D0
23	NanEye-D9	47	H012_TRIG_O
24	GPIO74	48	H1_INT

9. EOT FORM FACTOR BOARD LAYOUT AND SCHEMATIC

The current layout for the EoT form factor board can be seen in Figure 8-1. The board is planned FR4 1.55mm 8 layers with gold plated finishing. Layer stack is provided by the PCB supplier. Figure shows the front and rear views of the manufactured board. In addition, the break-off area can be seen in Figure 8-1 (a) on the left side of the board depicted by a vertical line (right side of P3 connector).



a



b

Figure 8-1: Manufactured EoT form-factor board: a) top view; b) rear view.

Following the preliminary high-level schematic that was presented in deliverable D2.5, the complete and finalised schematic for the validation version of the form factor board (R1M0E0) is presented here.

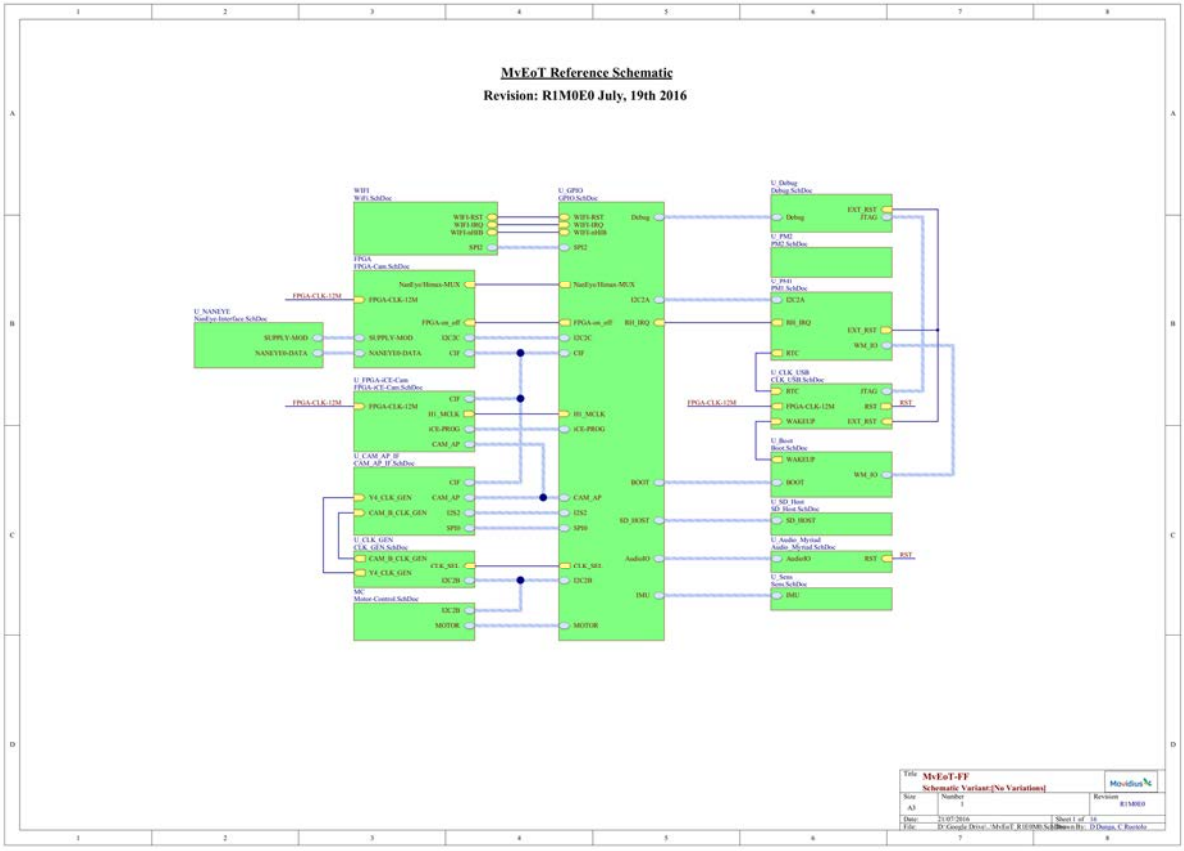


Figure 8-2: MvEoT_R1E0M0 schematic.

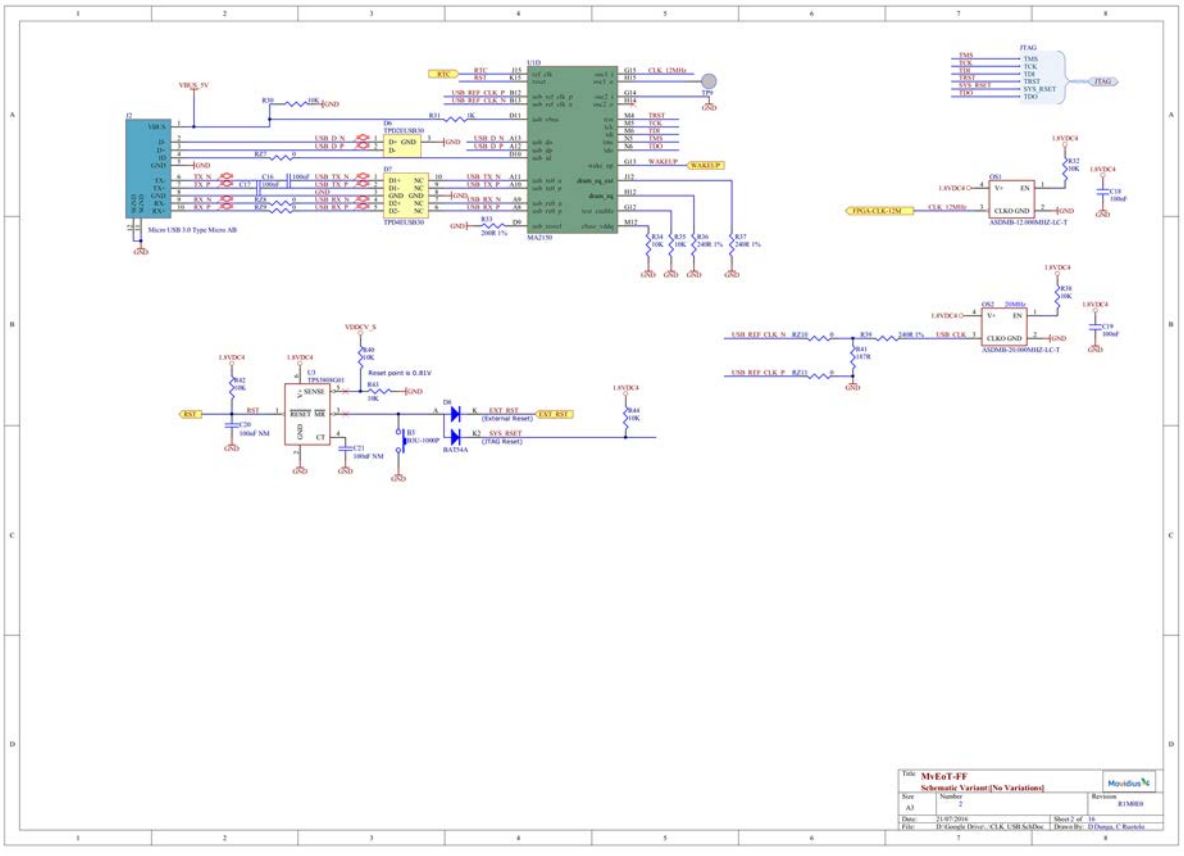


Figure 8-3: CLK_USB schematic document.

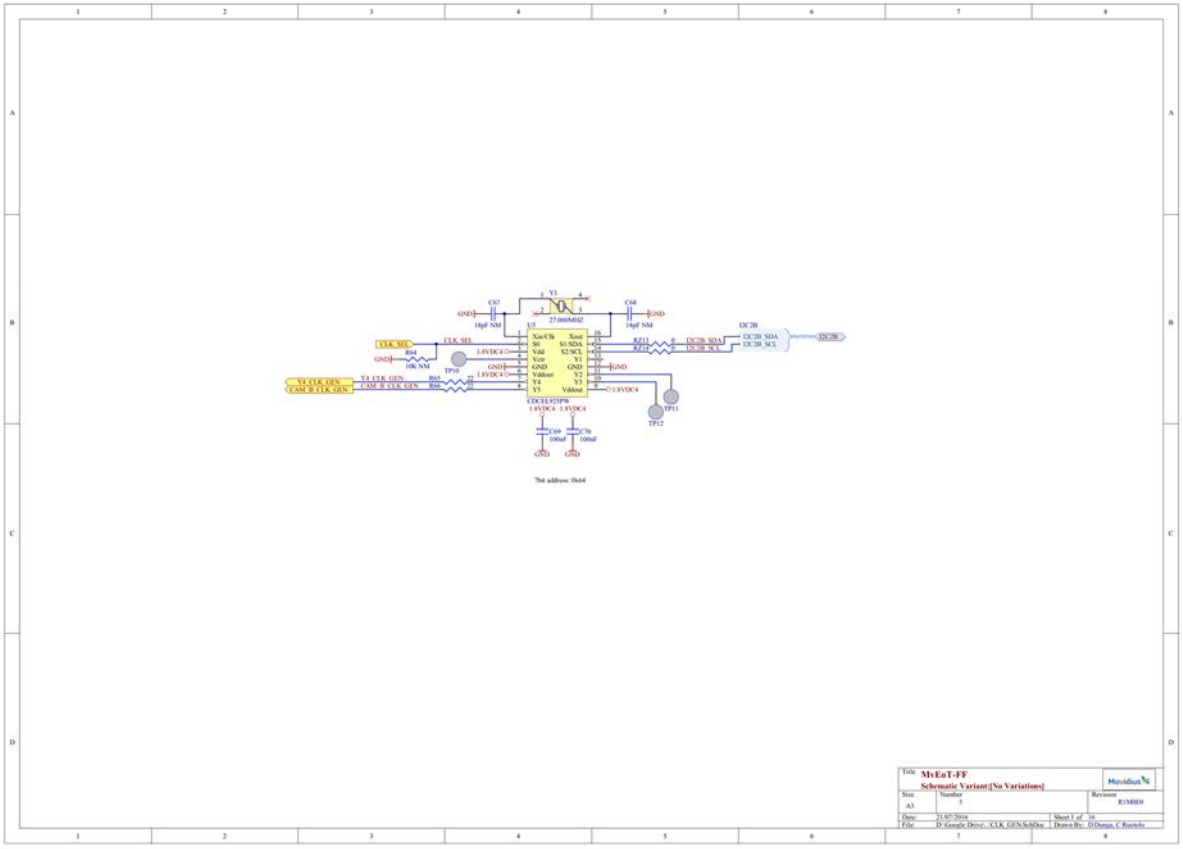


Figure 8-4: CLK_GEN schematic document.

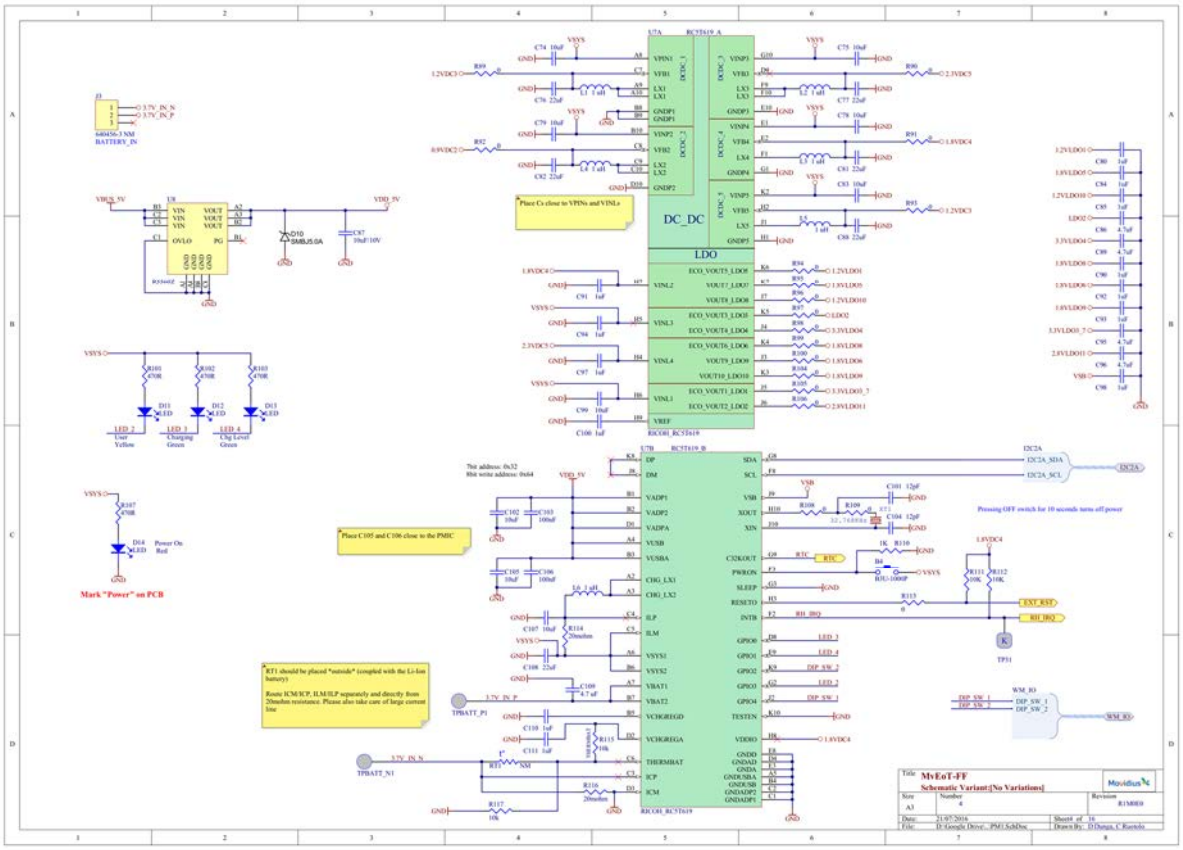


Figure 8-5: PMU schematic document.

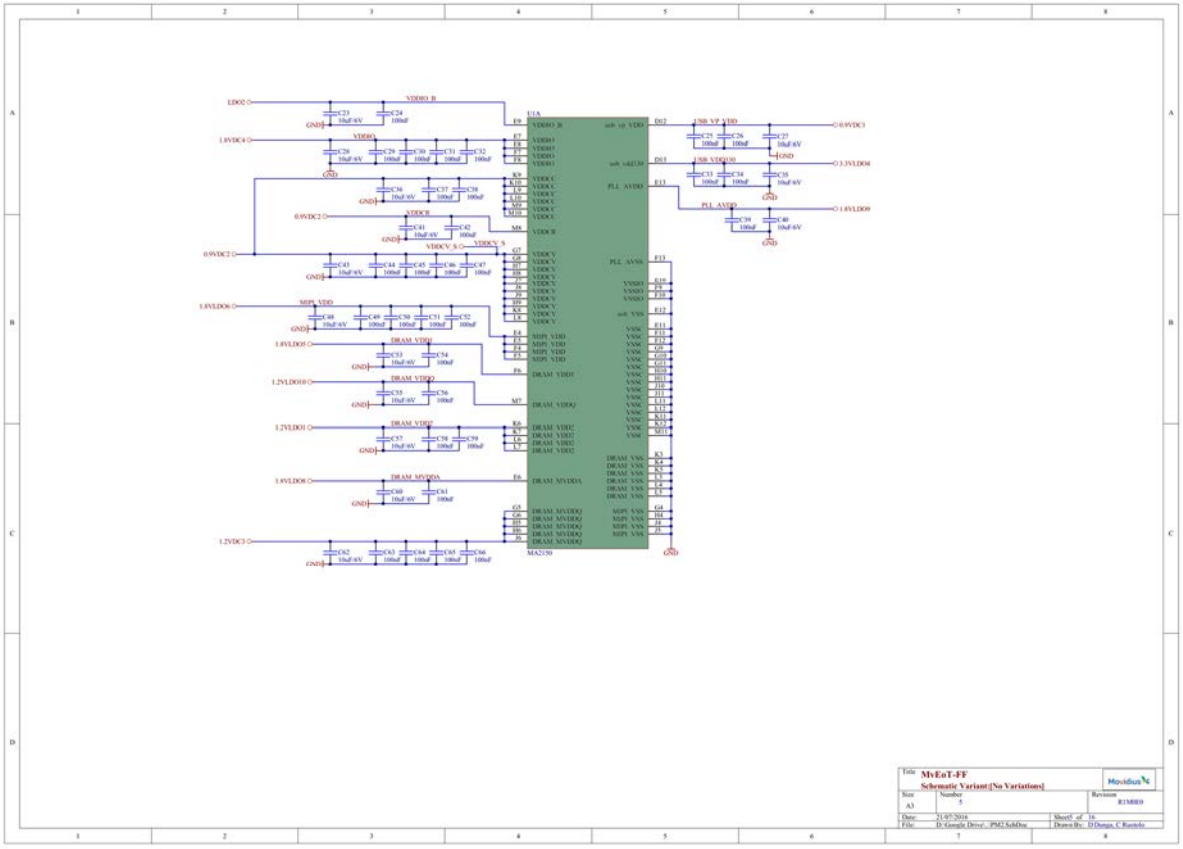


Figure 8-6: schematic document (cntd).

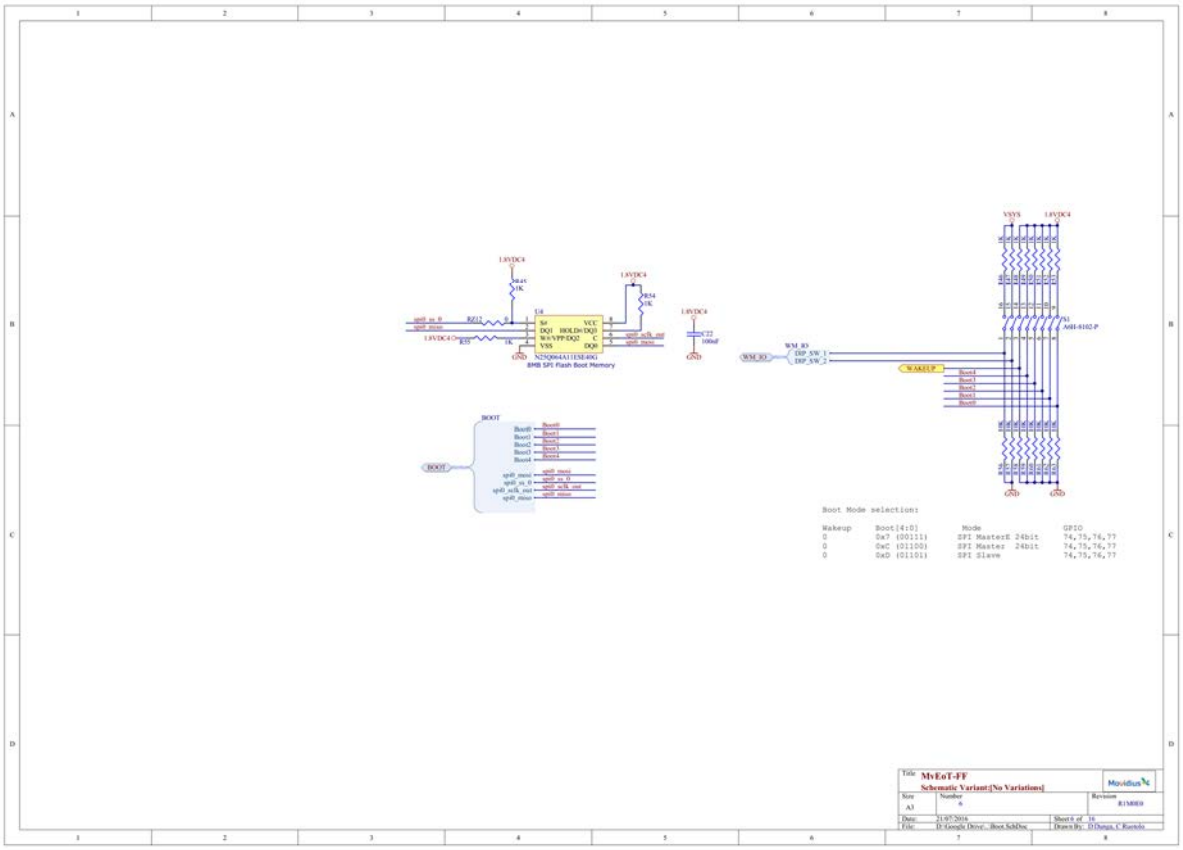


Figure 8-7: Boot schematic document.

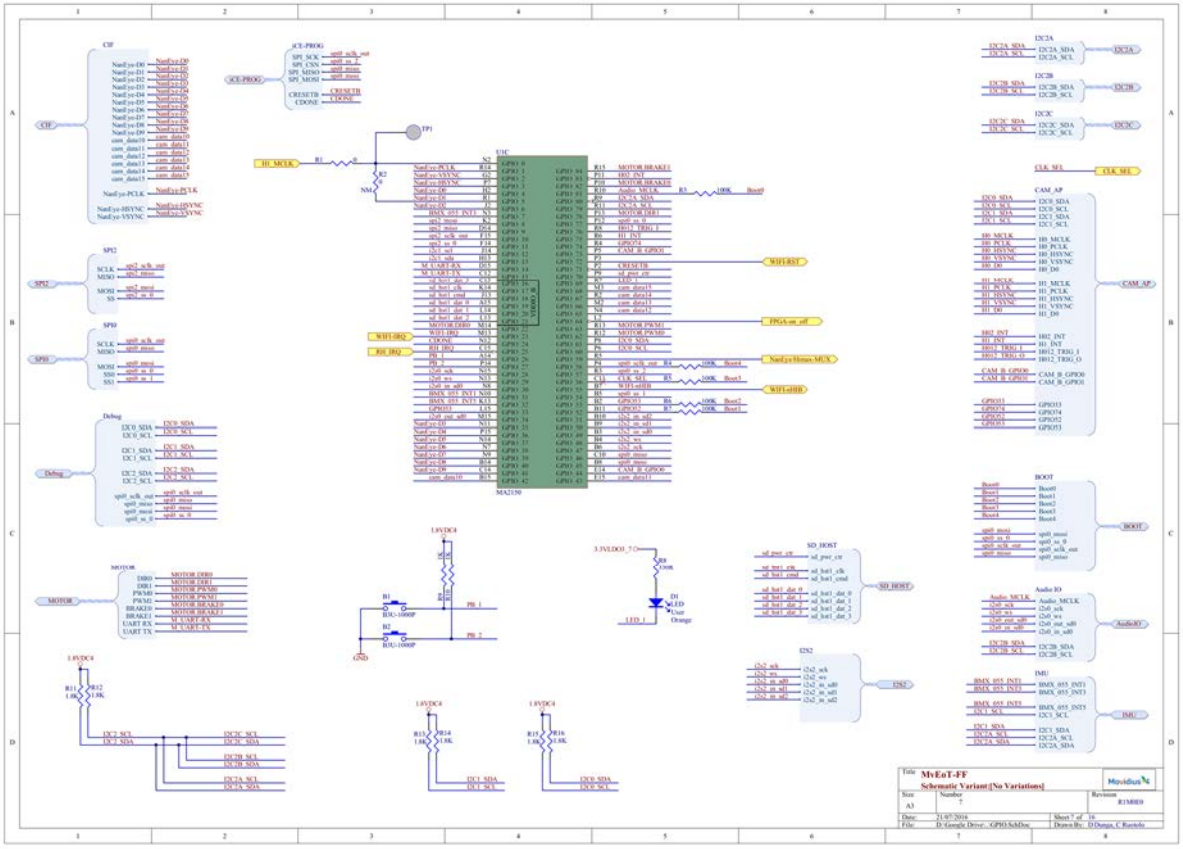


Figure 8-8: GPIO schematic document.

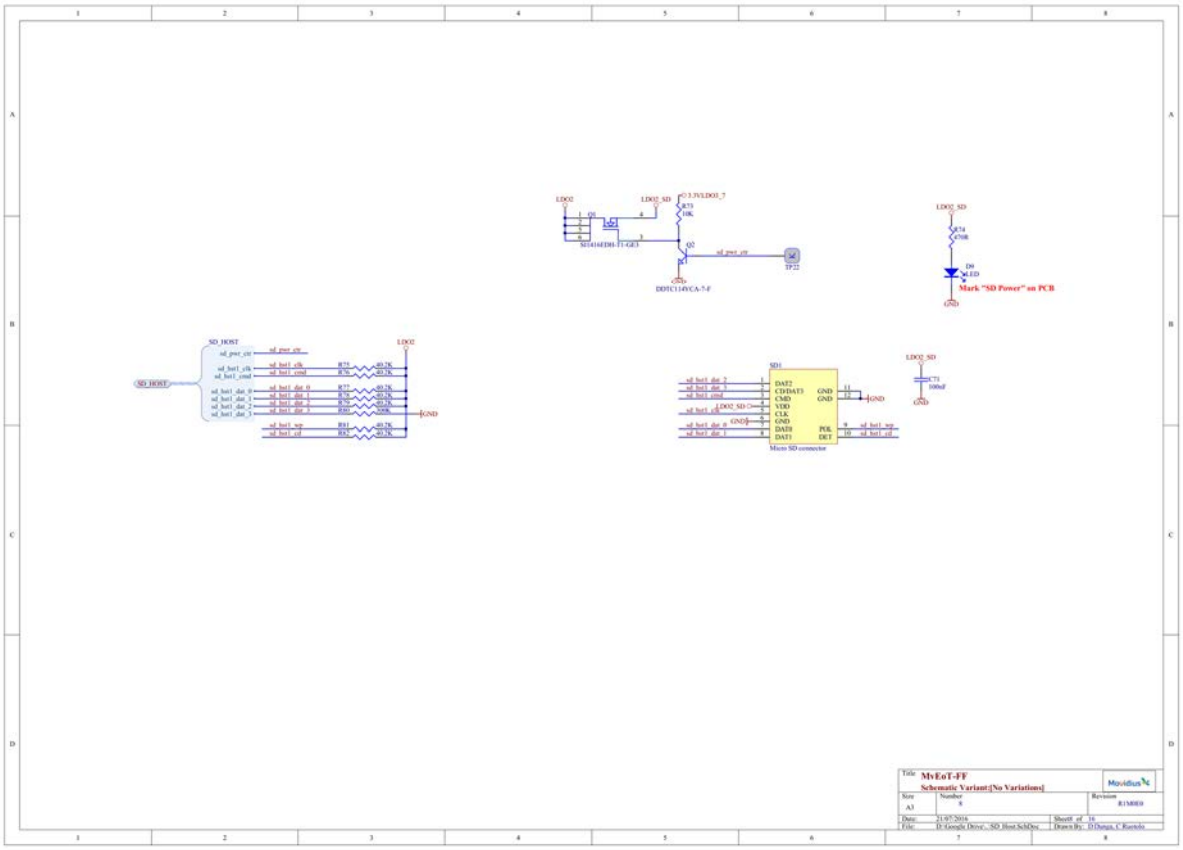


Figure 8-9: SD_Host schematic document.

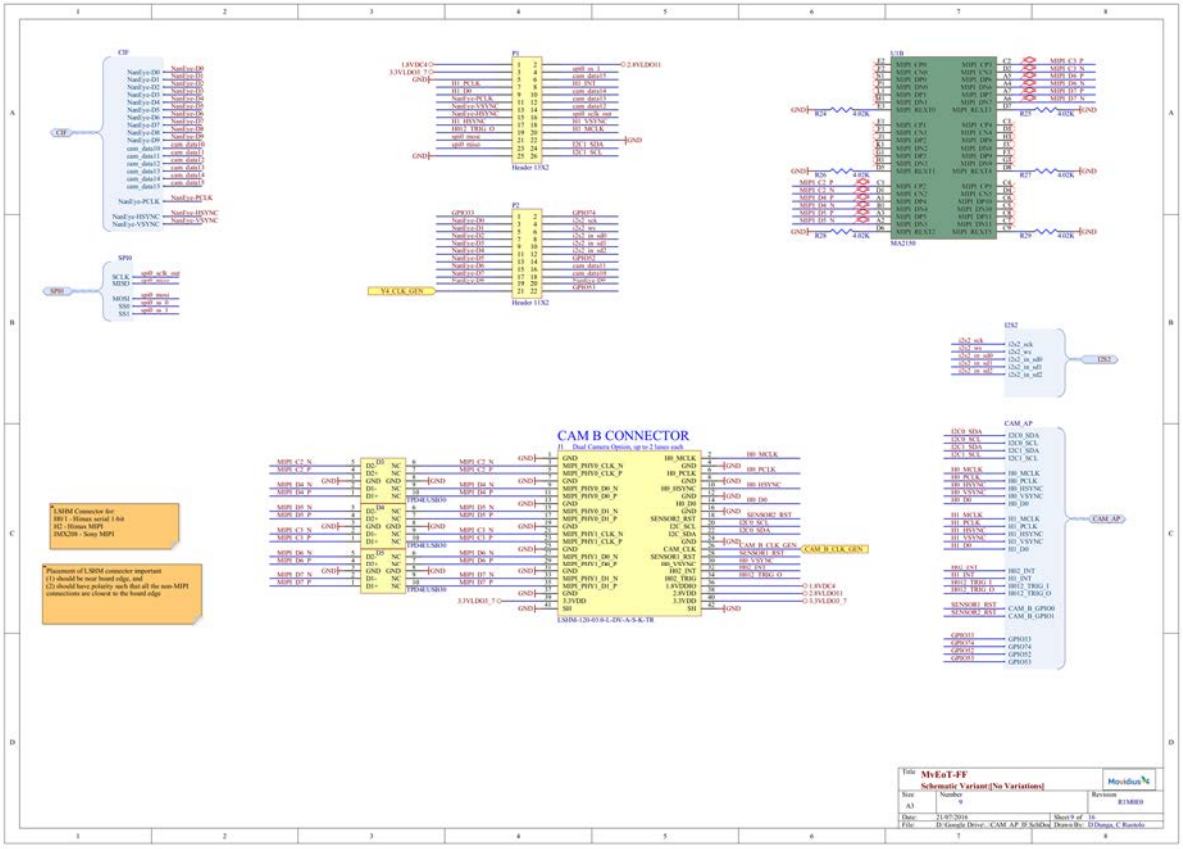


Figure 8-10: CAM_AP_IF schematic document.

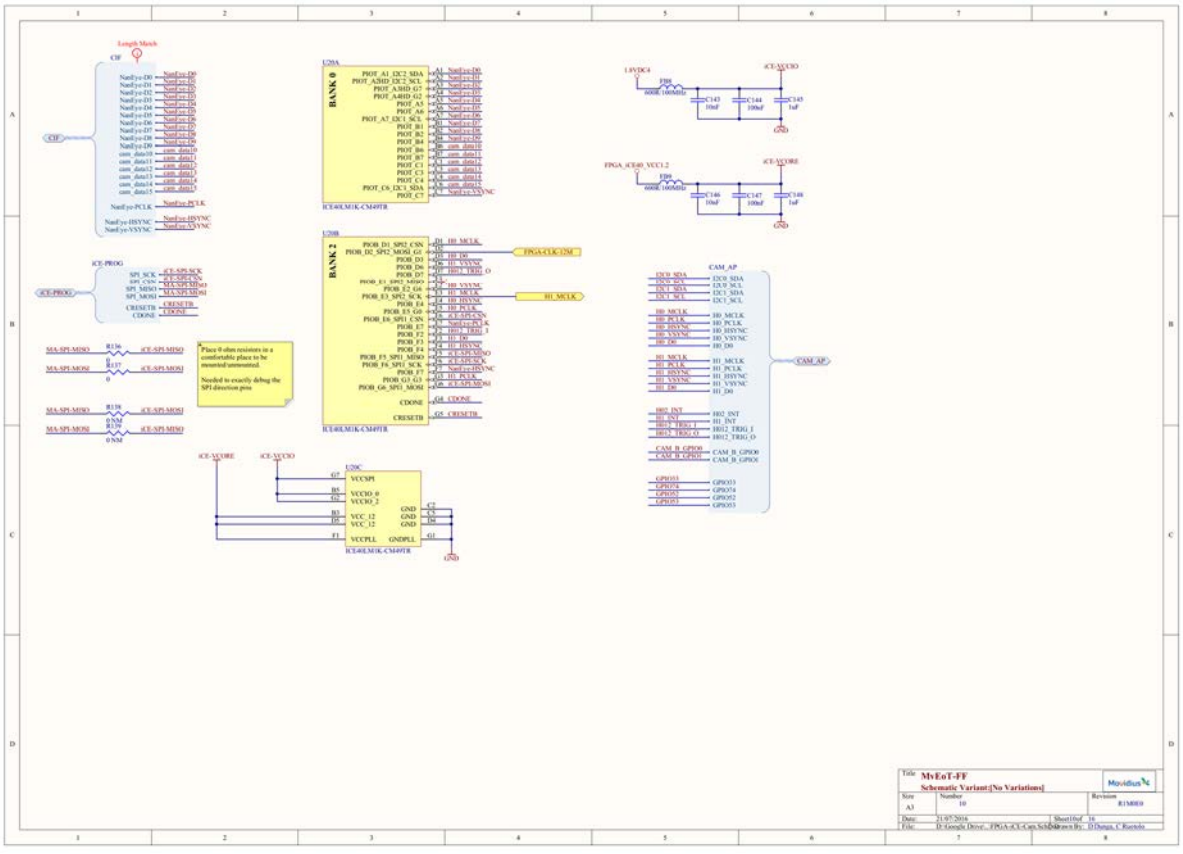


Figure 8-11: FPGA-iCE-Cam schematic document.

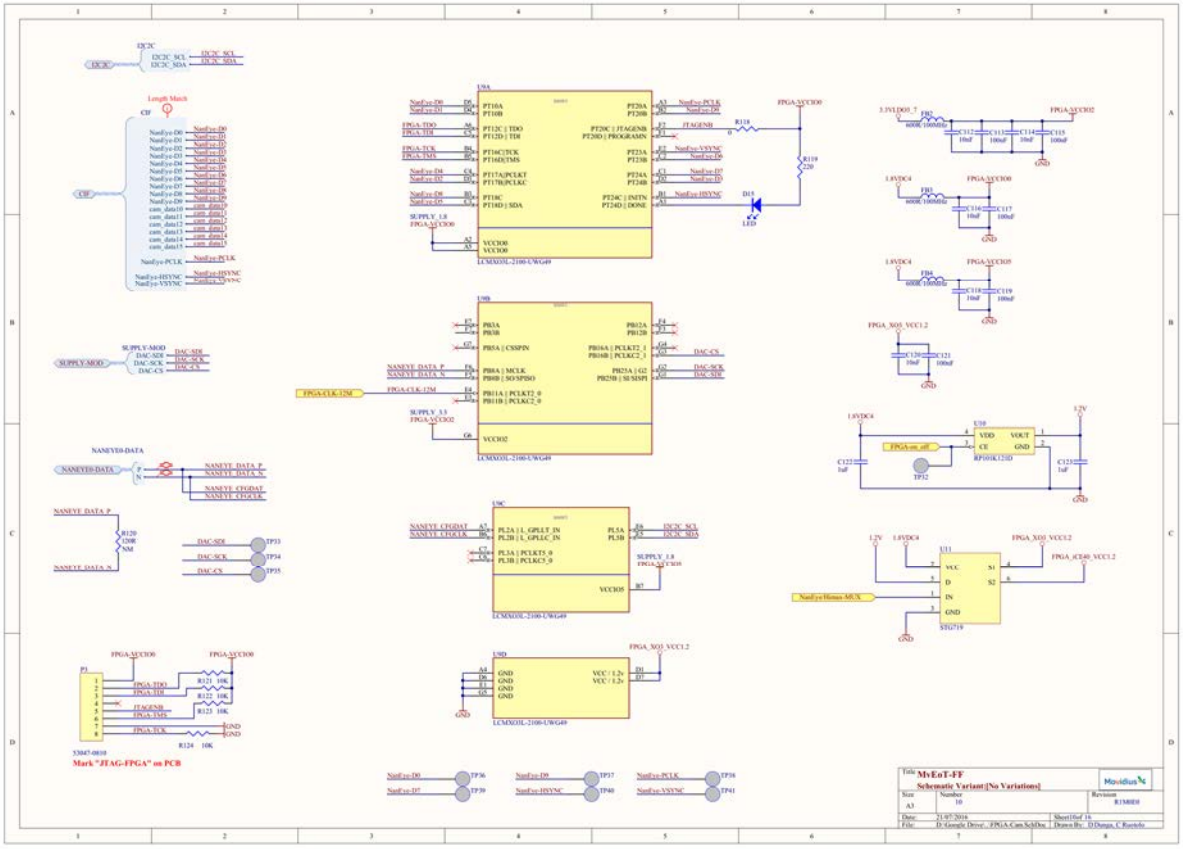


Figure 8-12: FPGA-Cam schematic document.

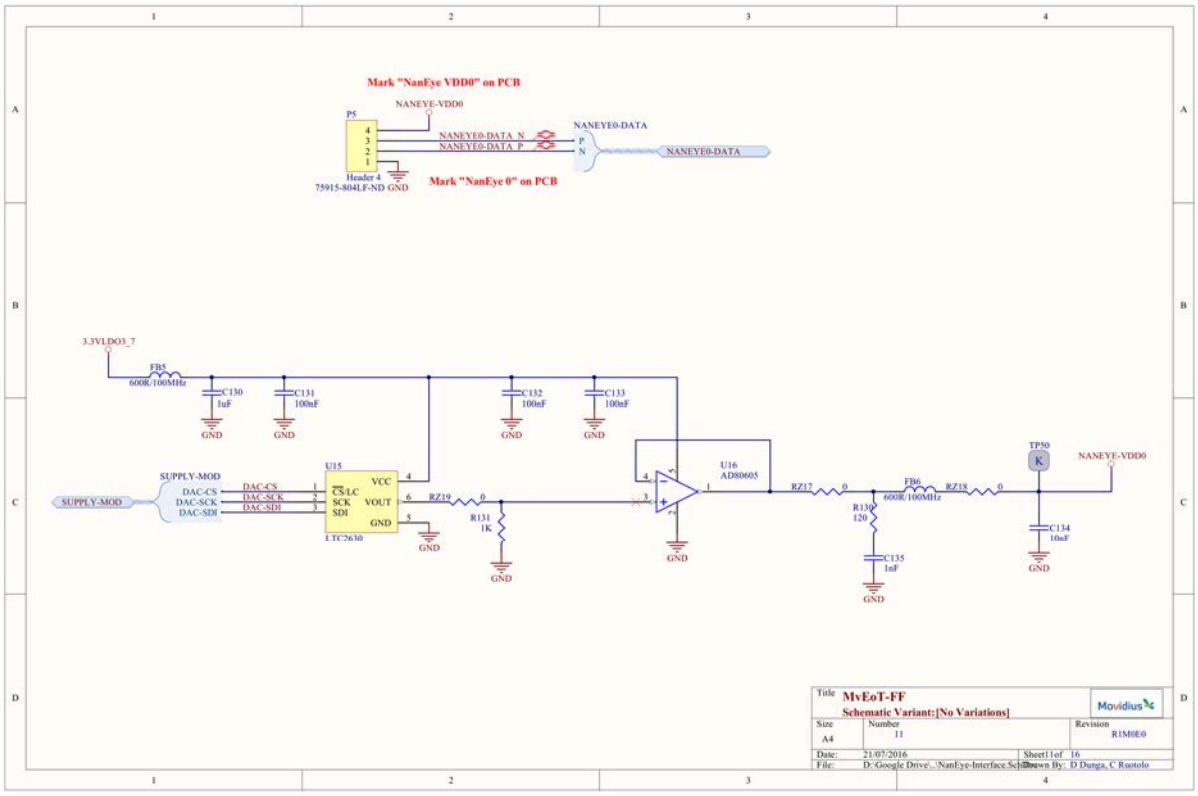


Figure 8-13: NanEye Interface schematic document.

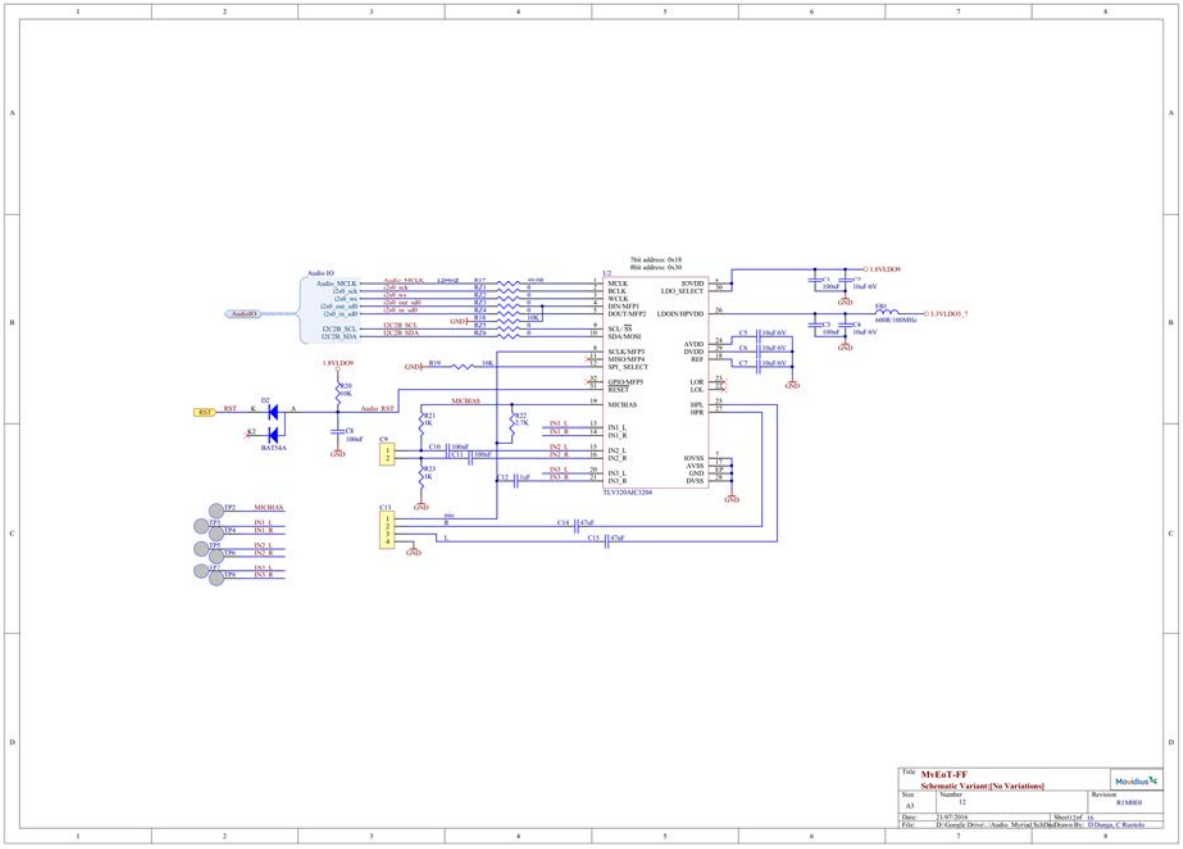


Figure 8-14: Audio Myriad schematic document.

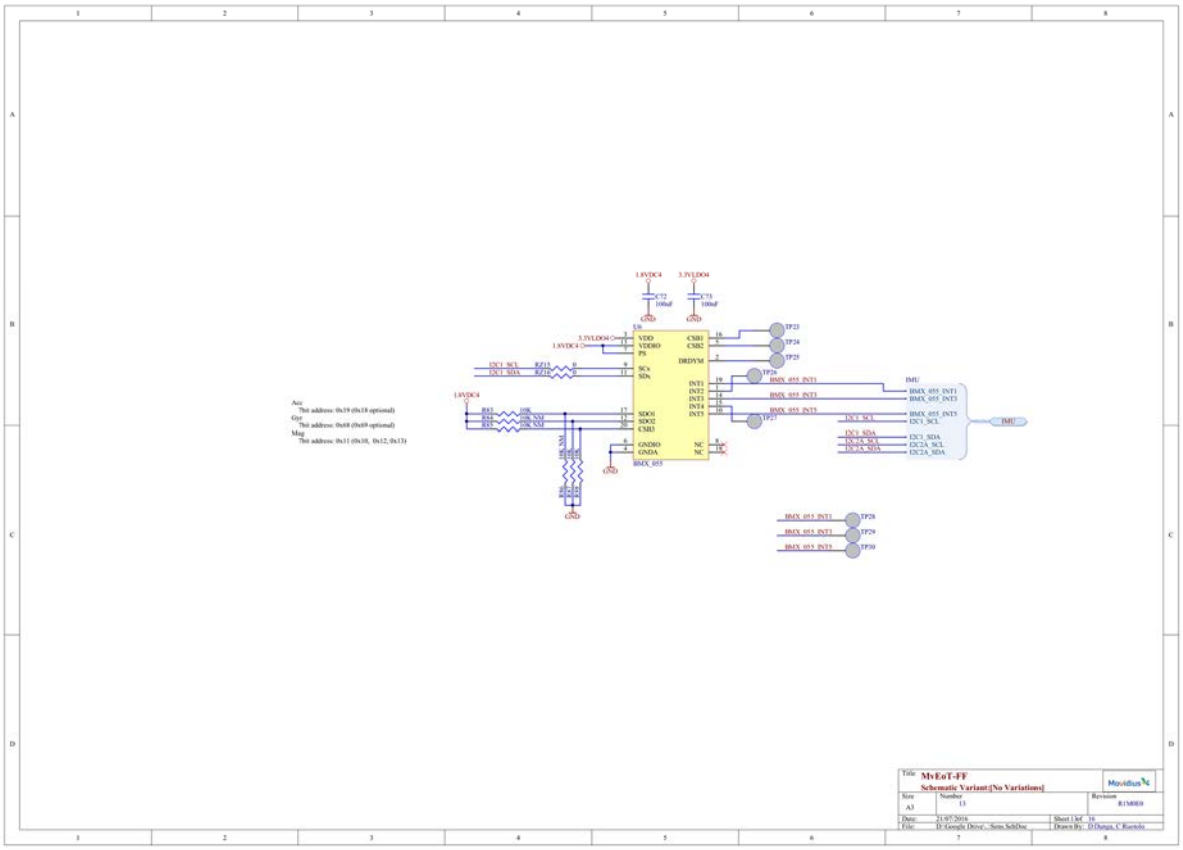


Figure 8-15: Sensors schematic document.

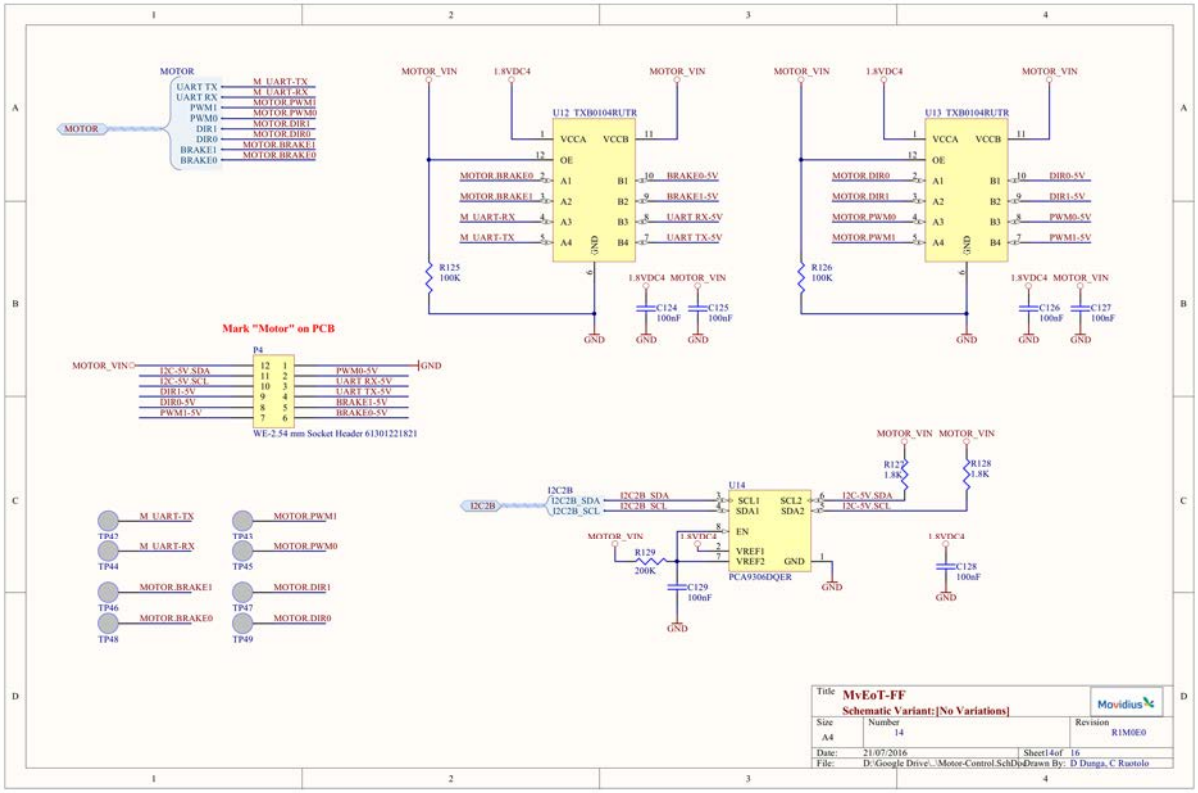


Figure 8-16: Motor-Control schematic document.

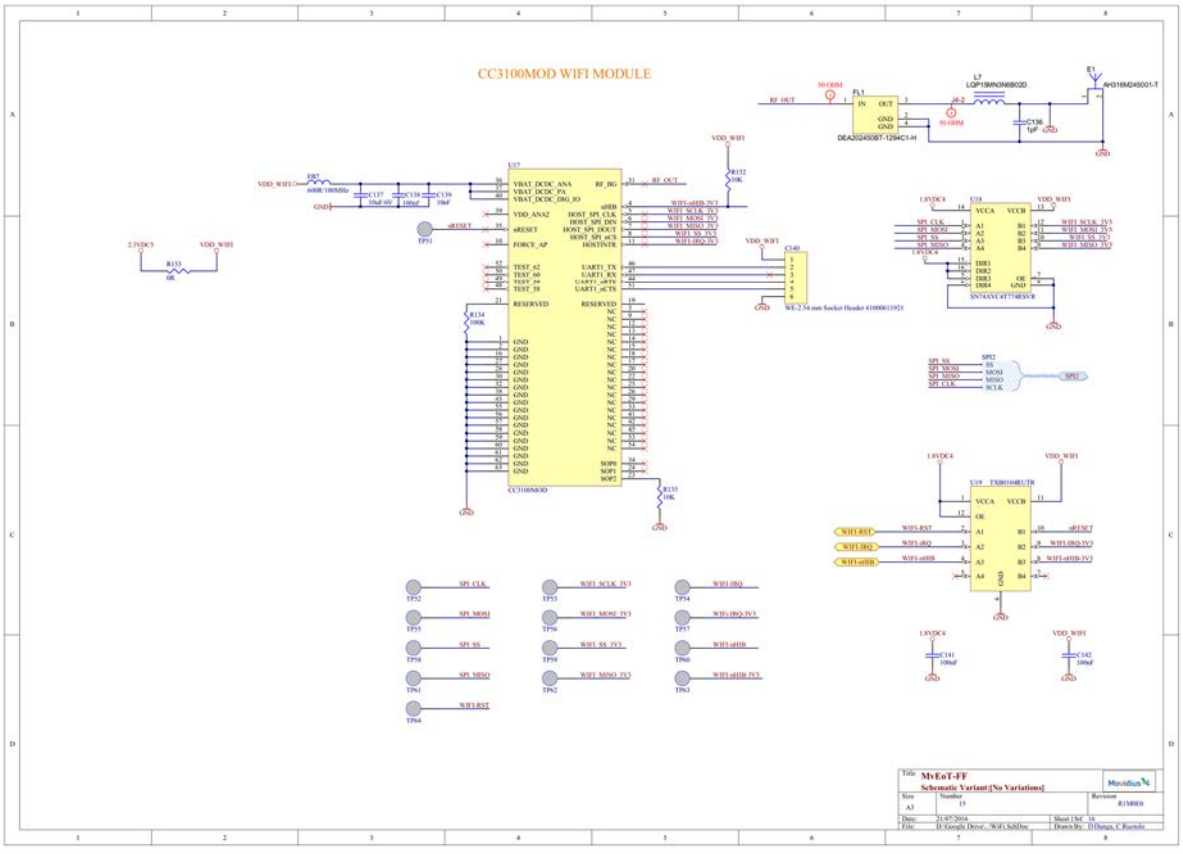


Figure 8-17: Wi-Fi schematic document.

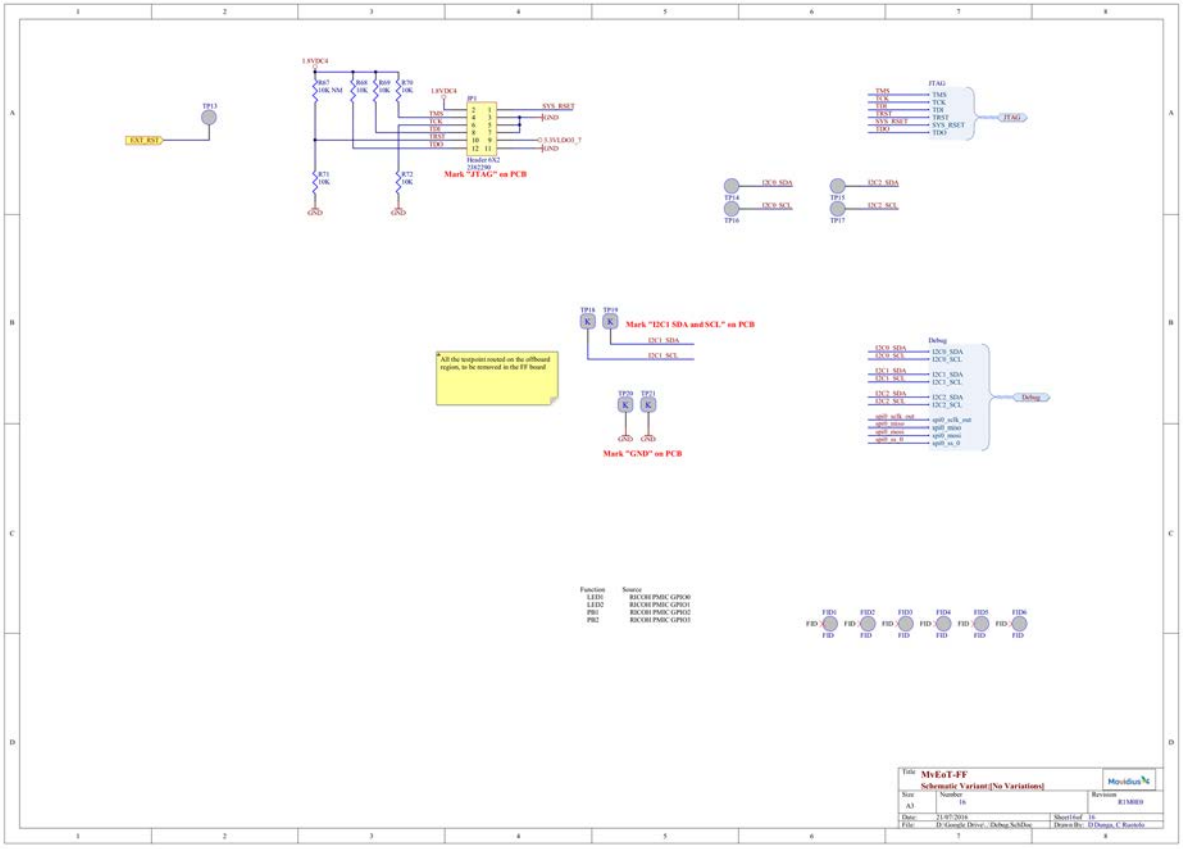


Figure 8-18: Debug schematic document.

10. EOT FORM FACTOR BOARD BOM

Comment	Designator	Description	Quantity
B3U-1000P	B1, B2, B3, B4	Tact Switch	4
100nF	C1, C3, C8, C9, C10, C11, C18, C19, C22, C24, C25, C26, C29, C30, C31, C32, C33, C34, C37, C38, C39, C42, C44, C45, C46, C47, C49, C50, C51, C52, C54, C56, C58, C59, C61, C63, C64, C65, C66, C71, C72, C73, C103, C106	Ceramic Capacitor SMD, Ceramic Capacitor SMD, Ceramic Capacitor SMD, Ceramic Capacitor SMD, Ceramic Capacitor SMD, Ceramic Capacitor SMD, Ceramic Capacitor SMD, Ceramic Capacitor SMD, Ceramic Capacitor SMD, Ceramic Capacitor SMD, Ceramic Capacitor SMD, Ce	44
10uF/6V	C2, C4, C5, C6, C7, C23, C27, C28, C35, C36, C40, C41, C43, C48, C53, C55, C57, C60, C62, C137	Ceramic Capacitor SMD	20
1uF	C12, C80, C84, C85, C90, C91, C92, C93, C94, C97, C98, C100, C110, C111, C123, C145, C148	Ceramic Capacitor SMD	17
47uF	C14, C15	Capacitor	2
100nF	C16, C17	Ceramic Capacitor SMD	2
100nF NM	C20, C21	Capacitor	2
10uF	C74, C75, C78, C79, C83	Ceramic Capacitor SMD	5
22uF	C76, C77, C81, C82, C88, C108	Ceramic Capacitor SMD	6
4.7uF	C86, C89, C95, C96	Ceramic Capacitor SMD	4
10uF/10V	C87	Ceramic Capacitor SMD	1
10uF	C99, C107	Ceramic Capacitor SMD	2
Cap Semi	C101, C138	Capacitor (Semiconductor SIM Model)	2
10uF	C102, C105	Ceramic Capacitor SMD	2
12pF	C104	Capacitor (Semiconductor SIM Model)	1
4.7 uF	C109	Ceramic Capacitor SMD	1
10nF	C112, C114, C116, C118, C120, C143, C146	Ceramic Capacitor SMD	7
100nF	C113, C115, C117, C119, C121, C124, C125, C126, C127, C128, C129, C131, C132, C133, C141, C142, C144, C147	Ceramic Capacitor SMD	18
1uF	C122	Ceramic Capacitor SMD	1
1uF	C130	Ceramic Capacitor SMD	1
10nF	C134, C139	Ceramic Capacitor SMD	2
1nF	C135	Ceramic Capacitor SMD	1
GRM1555C1H1R0BA01D	C136	CAP, CERM, 1 pF, 50 V, +/- 10%, C0G/NP0, 0402	1

LED	D1, D9, D11, D12, D13, D14, D15	LED	7
BAT54A	D2, D8	Diode dual common anode	2
TPD4EUSB30	D3, D4, D5, D7	ESD PROTECTION ARRAY, 4CH, SON-10	4
TPD2EUSB30	D6	DIODE, ESD, DUAL, USB3.0, SOT-3	1
SMBJ5.0A	D10	SMBJ5.0A	1
AH316M245001-T	E1	ANT BLUETOOTH W-LAN ZIGBEE WIMAX, SMD	1
600R/100MHz	FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9	inductance	9
DEA202450BT-1294C1-H	FL1	Multilayer Chip Band Pass Filter For 2.4GHz W-LAN/Bluetooth, SMD	1
LSHM-120-03.0-L-DV-A-S-K-TR	J1	Camera connector	1
Micro USB 3.0 Type Micro AB	J2		1
WE-1.27 mm Pin Header & Jumper 62100821021	J3	WR-PHD 1.27 mm Dual SMT Pin Header	1
WE-2.00 mm Pin Header 62000611121	J4	WR-PHD 2.00 mm Pin Header	1
WE-2.00 mm Pin Header 62000211121	J5	WR-PHD 2.00 mm Pin Header	1
Header 6X2	JP1	Header, 6-Pin, Dual row	1
1239AS-H-1R0M=P2	L1, L2, L3, L4, L5, L6	Inductor	6
LQP15MN3N6B02D	L7	Inductor, Film, 3.6 nH, 0.17 A, 0.5 ohm, SMD	1
ASDMB-12.000MHZ-LC-T	OS1	12Mhz Osc Module	1
ASDMB-20.000MHZ-LC-T	OS2	20MHz Osc Module	1
ASDMB-24.000MHZ-LC-T	OS3	12Mhz Osc Module	1
Header 13X2	P1	Header, 13-Pin, Dual row	1
Header 11X2	P2	Header, 11-Pin, Dual row	1
WE-2.00 mm Pin Header 62000811121	P3	WR-PHD 2.00 mm Pin Header	1
WE-2.54 mm Socket Header 61301221821	P4	WR-PHD 2.54 mm Dual Socket Header	1
Header 4	P5	Header, 4-Pin	1
SI1416EDH-T1-GE3	Q1	MOSFET N-CH SINGLE 30V 4A SO-8 PowerPAK	1
DDTC114YCA-7-F	Q2	NPN prebiased transistor	1
0	R1, R2, R113, R118, RZ1, RZ2, RZ3, RZ4, RZ5, RZ6, RZ7, RZ10, RZ11, RZ12	RESISTOR, RESISTOR, Resistor SMD, Resistor SMD, RESISTOR, RESISTOR, RESISTOR, RESISTOR, RESISTOR, RESISTOR, RESISTOR, RESISTOR, RESISTOR, RESISTOR	14
100K	R3, R4, R5, R6, R7, R134	RESISTOR	6
330R	R8	Resistor SMD	1

1K	R9, R10, R21, R23, R31, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R110	Resistor SMD	17
1.8K	R11, R12, R13, R14, R15, R16	Resistor SMD	6
49.9R	R17		1
10K	R18, R19, R20, R30, R32, R34, R35, R38, R40, R42, R43, R44, R56, R57, R58, R59, R60, R61, R62, R63, R64, R68, R69, R70, R71, R72, R73, R111, R112, R135	Resistor SMD	30
2.7K	R22	Resistor SMD	1
4.02K	R24, R25, R26, R27, R28, R29	Resistor SMD	6
200R 1%	R33	RESISTOR	1
240R 1%	R36, R37, R39	Resistor SMD, Resistor SMD, RESISTOR	3
187R	R41	RESISTOR	1
10K NM	R67	Resistor SMD	1
470R	R74, R101, R102, R103, R107	Resistor SMD	5
40.2K	R75, R76, R77, R78, R79, R81, R82	RESISTOR	7
300K	R80	Resistor SMD	1
10K	R83, R87, R88, R121, R122, R123, R124, R132	Resistor SMD	8
10K NM	R84, R85, R86	Resistor SMD	3
zero ohm jumper	R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100, R104, R105, R106, R108, R109	Resistor	17
Current Sense Resistors	R114, R116, R117	Current Sense Resistors	3
THERMBAT	R115	Resistor Thick Film	1
220	R119	Resistor SMD	1
120R	R120	Resistor SMD	1
100K	R125, R126	Resistor SMD	2
1.8K	R127, R128	Resistor SMD	2
200K	R129	Resistor SMD	1
120	R130	Resistor SMD	1
1K	R131	Resistor SMD	1
0R	R133	RESISTOR	1
0	R136, R137	Resistor SMD	2
0 NM	R138, R139	Resistor SMD	2
Res Thermal	RT1	Thermistor	1
0	RZ8, RZ9	RESISTOR	2
0	RZ15, RZ16, RZ17, RZ18, RZ19	RESISTOR	5
A6H-8102-P	S1	Ultra-Low Profile, Half-Pitch, SM, Slide DIP Switch, Flat Actuator,	1

		White Striker, 8 Position, SPST, Seal Tape: Embossed Taping Model	
Micro SD connector	SD1	Molex MicroSD socket	1
TP	TP18, TP19, TP20, TP21, TP22, TP31, TP50	Keystone TEST POINT	7
MA2150	U1	MA2150	1
TLV320AIC3204	U2	Audio Converter	1
TPS3808G01	U3	IC Voltage monitoring	1
N25Q064A11ESE40G	U4	IC FLASH 64MBIT 108MHZ	1
BMX_055	U6	BMX055 9-axis sensor module	1
RICOH_RC5T619	U7	PMIC	1
R5560Z	U8	Overvoltage Protection Switch IC	1
LCMXO3L-2100-UWG49	U9	Lattice MachXO3 Series FPGA Family, 2112 Logic Cells, 1.2 V Core, 74 K Embedded RAM Bits, 49-Ball WLCSP	1
STG719	U11	Low Voltage SPDT Switch	1
TXB0104RUTR	U12, U13, U19	4-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR	3
PCA9306DQER	U14	Dual Bi-Directional I2C-Bus and SMBus Voltage Level-Translator, 0 to 5.5 V, -40 to 85 degC, 8-pin X2SON (DQE), Green (RoHS & no Sb/Br)	1
LTC2630	U15	Single 12-bit DAC w/ 2.5V Ref, Rail-to-Rail, Power on at Zero	1
AD80605	U16	Low Noise Rail-to-Rail Single-Supply Op Amp	1
CC3100MOD	U17	SimpleLink Wi-Fi module	1
SN74AVC4T774RSVR	U18	4-Bit Dual-Supply Bus Transceiver	1
ICE40LM1K-CM49TR	U20	iCE40 LM1K Series FPGA Family, 1100 Logic Cells, 1.2 V Core, 64 K Embedded RAM Bits, 49-ball ucBGA, Pb-Free, Tape and Reel	1
32.768KHz	XT1	CRYSTAL FC-12M, 32.768 KHZ, 9 PF	1
TOTAL			378

11. CONCLUSIONS

In this report, the EoT final factor-form board was presented. The device consists of a custom designed (between 30x15mm and 45x20mm) 10-layer (2 layers of which for debugging) high density PCB that is optimised for size and power efficiency. As the core of the device, the Myriad2 MA2150 VPU controls all processing and peripherals. The device supports a number of visual sensors including a 1x1x1.7mm NanEye2D sensor from Awaiba as the primary visual sensor, which is capable of capturing 250x250 pixel images. NanEye2D is a module package CMOS image sensor and integrated lens that is fully self-timed, consuming less than 5mW at 60 frames per second (fps). A high-resolution Sony IMX208 1080P MIPI sensor also is available on the board in case the user wants to acquire higher resolution images. A Himax HM01B0 sensor with 240x320 pixel images provides the user with another low-power image acquisition sensor. This sensor communicates with Myriad2 over different protocols from single line data accessible even through I2S and SPI to 4-line nibble data which is converted into CIF data using an FPGA device such as the iCE40. The EoT form factor device is capable of simultaneously acquiring the images from multiple camera which is an interesting functionality for applications such as drones.

Additional peripherals such as a tri-axial gyroscope, tri-axial accelerometer, magnetometer, and microphone enable a cascade filtering approach for 'interesting' event detection and reaction. Since all the processing is done in house with Myriad2 and also to prevent the highly power consuming image streaming over the Wi-Fi, decisions coupled with relevant metadata, based on the sensor data and the information extracted from visual processing and neural inference, can be communicated over an integrated Wi-Fi module to external devices or to the cloud. In personal assistant use-cases, audio cues for prompting and notification are enabled via a full on-board audio codec. Integrated level shifters expose motor control pins for direct, yet generic, robotic control (GPIOs, PWMs, I2C, and UART) without the need for external components.

By combining Myriad2, NanEye, low-power board design and energy efficient component selection, the EoT platform can run for up to 24 hours from a fully charged Lithium-ion Polymer (Li-Po) battery. USB and micro-SD functionality support rapid development and data logging modalities.

12. GLOSSARY

AON	Always ON
AP	Access Point
API	Application Programming Interface
BGA	Ball Grid Array
BOM	Bill of Materials
BRISK	Binary Robust Invariant Scalable Keypoints
BSD	Berkeley Software Distribution
CISC	Complex Instruction Set Computing
CNN	Convolutional Neural Network
CSS	CPU Subs-System
CSP	Chip Scale Package
DDR	Double Data Rate
DIP	Dual in-line Package
DMA	Direct Memory Access
DSS	DDR Sub-System
DoW	Description of Work
FPGA	Field-Programmable Gate Array
GPIO	General Purpose Input/Output
GPL	General Public License
HD	Hard Disk
HOG	Histogram of Oriented Gradients
HTTP	Hypertext Transfer Protocol
HW	Hardware
I2C	Inter-Integrated Circuit
I2S	Integrated Interchip Sound
IO	Input/Output
ISR	Interrupt Service Routine
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
LED	Light-Emitting Diode
LK	Lucas-Kanade
MAC	Media Access Control
MDK	Movidius Development Kit
MIPI	Mobile Industry Processor Interface
MQTT	Message Query Telemetry Transport
MSS	Media Sub-System
MvCv	Movidius Computer Vision
OS	Operating System
PC	Personal Computer
PDF	Portable Document Format
PMB	Processor Memory Block
PMU	Power Management Unit
PNG	Portable Network Graphics
POSIX	Portable Operating System Interface
QR	Quick Response
REST	Representational State Transfer
RISC	Reduced Instruction Set Computing

RTEMS	Real-Time Executive for Multiprocessor Systems
RTP	Real-Time Transport Protocol
RTSP	Real-Time Streaming Protocol
SD	Secure Digital
SIFT	Scale-Invariant Feature Transform
SoC	System on Chip
SPI	Serial Peripheral Interface
SVM	Support Vector Machines
SW	Software
TCP/IP	Transmission Control Protocol / Internet Protocol
TI	Texas Instruments
ULPIS	Ultra-Low Power Image Sensor
VPU	Vision Processing Unit
WAV	Waveform Audio File
WEP	Wired Equivalent Privacy
WPA	WiFi Protected Access

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