Horizon 2020 PROGRAMME

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D2.2

Image Sensor Description



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4. ABSTRACT

The image sensor imbues the EoT device with 'eyes' and hence is a key component in the overall EoT project. Power is the primary driver in the selection of the sensor, where a very low power budget is essential for battery powered wearable devices. The NanEye2D image sensor from Awaiba is a small form-factor, low-power sensor designed for medical endoscopy applications. It delivers a 250x250 image at 44 frames per second over a 4 wire interface. Additional logic for deserialising the pixel data and interfacing the sensor to the Myriad processor is incorporated on an FPGA.

5. IMAGE SENSOR

Introduction



Fig 5.1: NanEye 2D image sensor

The NanEye sensor (Awaiba, Portugal), shown in Fig. 5.1, is an extremely small module package incorporating a CMOS image sensor and an integrated lens. The sensor is fully self-timed so that once it is powered on it continually transmits image data in rolling shutter mode. Sensor properties including framerate, analogue gain and exposure that can be configured by external logic. The NanEye is designed for medical endoscopy applications, where the sensor is distal by up to 2 metres from the receiving circuitry, and where illumination is provided by an accompanying light source. The principal properties of the sensor are provided in Table 5.1.

Resolution	250x250 pixels (62.5kP)
Pixel size	3 x 3 um
Pixel depth	10 bit
Shutter type	Rolling shutter
Frame rate	44 FPS

Table 5.1: Summary	of NanEye Sensor Specifications

Data output	Proprietary 10 bit digital LVDS
Chroma	RGB
Power consumption	4.2 mW @ 2.1V nominal supply
Operating temperature	0-60 degrees
Responsivity	8 DN/nJ/cm ²
Full well capacity	10ke-
Dynamic range	42dB
FPN/PRNU	<0.5%/<1% software corrected)
Temporal noise dark	1.2DN rms
Footprint	1.0 x 1.0 x 1.7 mm

Form factor

With a total volume of 1.7 mm³ the NanEye provides an extremely small, yet fully integrated, imaging solution. The custom lens bonded to the sensor is F2.8 with a 120 degree field of view. Owing to its design as an endoscopic camera, the depth of focus is between 5.0 and 35.0 mm. This extremely close focus may lead to some challenges in image processing for the EoT use cases where scene depths are typically much larger (up to room scale). NanEye frame data can be transferred up to 2m over the attached 4 wire LVDS cable.

Power

The NanEye is supplied with a DC voltage between 1.8V and 2.4V. Varying the voltage within this range varies the frame rate of the sensor, as shown in Fig. 5.2 (Blue - typical; Red- min and max). When supplied with a nominal 2.1V, the sensor consumes 4.2mW. EoT applications will benefit from such low power consumption, and will enable the use of the NanEye as an 'always on' sensor.



Figure 5.2: Relationship between framerate and supply voltage

Modulation of the NanEye power supply is achieved via a DAC controlled over I2C from an FPGA. Figure 5.3 shows the schematic for the recommended power supply and modulation circuit. In addition to enabling a small variation of the frame rate, high frequency supply voltage modulation is used to eliminate image artefacts that can appear in images from the sensor.



Figure 5.3: NanEye power supply incorporating modulation

Interface

The NanEye sensor is bonded to a 4 wire interface, consisting of supply voltage, ground and two serial LVDS data signals. Fig. 5.4 shows the physical interface on the distal end of the NanEye. The LVDS signals are robust to noise whilst being suitable for fast decoding via a comparator.



Figure 5.4: NanEye physical interface

Frame pixel data is transferred serially with embedded clock over these LVDS datapaths. Sensor configuration is performed on the LVDS datapaths by time sliced modulation. After each frame is transferred from the sensor an upstream configuration phase is initiated in which configuration data can be written to the sensor. During this phase the LVDS datapaths are used for serial clock and serial data transmission. After a predefined time slice, the interface reverts to downstream pixel data transmission and the next frame is transferred.

On the EoT DevBoard (also known as Rev1), the Movidius Myriad processor is configured to receive the NanEye image data over a parallel CIF (Camera InterFace) interface. Hence the serial pixel data must be decoded and then deserialised before transmission to the Myriad. This task is performed by a Lattice MachXO3 FPGA. Two modes are possible for interfacing the NanEye to the Myriad via the FPGA, and for evaluation and verification purposes both of these modes are implemented on the EoT DevBoard.

5.4.1. Mode A

In Mode A the LVDS data is transmitted directly to a differential receiver on the FPGA. Fig. 5.5 shows the relevant schematic. The FPGA decodes the resulting single ended data, deserialises it to 10 bit parallel format, and then retransmits it over 1.8V parallel CIF to the Myriad. For sensor configuration, the FPGA receives configuration data from the Myriad over I2C, and reformats this for transmission as clock and data signals (at NanEye supply voltage, VCC) over the LVDS pair to the NanEye. During configuration, the differential receiver on the FPGA is tristated, and during pixel data transfer the configuration outputs on the FPGA are tri-stated.



Figure 5.5: NanEye to FPGA Mode A interface

5.4.2. Mode B

In Mode B the LVDS data is input to a discrete fast comparator, which outputs single ended data that is input to the FPGA. See Fig. 5.6 for the interface schematic. As with Mode A the FPGA decodes this data, deserialises it to 10 bit parallel format, and then retransmits it over 1.8V parallel CIF to the Myriad. For sensor configuration, the Myriad sends the configuration data to the FPGA via I2C, and the FPGA reformats and outputs this data to a signal translator. The signal translator shifts the clock and data voltages to VCC for transmission to the NanEye. During pixel data transfer the signal translator component is disabled (via the FPGA).



Fig. 5.6: NanEye to FPGA Mode B interface

In both modes of operation the FPGA also decodes the frame breaks and transmits the appropriate vertical and horizontal timing signals (VSYNC and HSYNC) to the Myriad, as well as the pixel clock (PCLK).

Both Mode A and Mode B were verified on the EoT DevBoard. Due to the smaller component count and simpler board layout, Mode A was chosen for the EoT form factor board development. Fig. 5.7 shows a block diagram of this chosen interface.



Figure 5.7: NanEye – FPGA – Myriad interface overview

Image parameters

The NanEye is a rolling shutter image sensor with a resolution of 250 x 250 pixels. The low pixel resolution of the NanEye may present some challenges for object/activity detection/recognition in EoT. However, as part of a cascade filter approach this resolution is expected to be sufficient. Besides, Awaiba is at the time of writing working on an enhanced model.

5.5.1. Sensor Configuration

A 16 bit register on the NanEye stored the sensor configuration and can be written to during the upstream configuration phase. The bit assignment of this register is shown in Table 5.2.

- *vref_cds* is a two bit value that can be used to adjust the reset offset, but it is recommended that it be kept at its default value.
- *vrst_pixel* is a two bit value describing the reset voltage of the pixels. Higher values correspond to higher linear response range but may lead to non-linear sensor behaviour. Lower values produce a lower linear swing and lower saturation output.
- *offset* is a two bit value that determines the black level of the sensor (pixel voltage corresponding to 0 output).
- *inverse_gain* is a two bit value that controls the gain of the on-sensor ADC. It should be set to the lowest value that permits signal saturation.
- *rows_in_reset* is an 8 bit value that controls the exposure.

The NanEye implements a rolling shutter that can be directly controlled by specifying the number of rows in reset (and hence not being exposed) for any

given frame. Photons are only integrated for pixels that are in the integration state - charge does not accumulate on pixels in the reset state. As shown in Fig. 5.8, the number of rows in the integration state is the total rows minus the number of rows in reset. For a nominal frame rate of 44 FPS, the exposure is thus variable between approximately 184us and 23ms.

Register bit	Function	Default value
15	vref_cds[1]	1
14	vref_cds[0]	0
13	vrst_pixel[1]	1
12	vrst_pixel[0]	0
11	offset[1]	0
10	offset[0]	1
09	inverse_gain[1]	1
08	inverse_gain[0]	0
07	rows_in Reset[7]	0
06	rows_in Reset[6]	0
05	rows_in Reset[5]	0
04	rows_in Reset[4]	0
03	rows_in Reset[3]	0
02	rows_in Reset[2]	0
01	rows_in Reset[1]	1
00	rows_in Reset[0]	0

 Table 5.2: NanEye configuration register



Figure 5.8: Operation of NanEye rolling shutter exposure

Spectral Response

The NanEye 2D sensor used in the EoT project is an RGB Bayer version of the sensor, with spectral responsivity as shown in Fig. 5.9. The Bayer format is GRBG. Debayering must be performed as part of the image signal processing pipeline.



NanEye Relative Spectral Response Color Version



EoT DevBoard

There are two headers for connecting NanEye sensors to the EoT DevBoard. For each of these headers, a connected sensor can be configured to operate in either Mode A or Mode B via appropriate removal of 0 ohm resistors. After completing board testing and NanEye interface verification for all modes, the EoT DevBoards were configured for a NanEye sensor (in Mode A) connected to the NanEye1 header, as shown in Fig. 5.10.

Example NanEye Images

Fig. 5.11 shows sample images captured with the NanEye sensor in indoor and outdoor environments. These images have been processed through Awaiba's standard image processing pipeline, which includes debayering, gamma correction and colour correction.



Figure 5.10: NanEye connection on EoT DevBoard



Figure 5.11: Sample debayered images from NanEye sensor (after basic image processing)

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